SECTION 4

CIRCUIT BOARDS AND THEORY OF OPERATION

4.0 GENERAL

This section addresses each circuit board of the Model 115 Fetal Monitor and its respective Theory of Operation. To facilitate understanding, applicable diagrams and schematics have been referenced.

4.1 PC BOARD OVERVIEW

The following summaries address the major function of each PC board found in the card cage. Refer to DIAGRAMS 11-1 (single-cardiotach) and 11-2 (dual-cardiotach).

BOARDS IN CARD CAGE:

(Common Boards)

MULTIFUNCTION BOARD (5800)

The US circuitry generates a 2.3 MHz transmit signal and also receives, amplifies, and detects the return signal. An audio signal is then sent to the Correlator Board.

The UA circuitry (toco and strain-gauge) contains a preamp which provides the CPU Board with a frequency output proportional to the input signal.

The PHONO filtering and amplification circuitry provides 80 Hz audio signals to the Correlator Board for heartbeat detection. The Correlator Board returns AGC'd phono which is then squared and sent to the audio amplifier.

The audio amplifier drives the speaker with PHONO or US audio tones or with 1.1-kHz beeps for ECG mode heartbeats.

POWER SUPPLY BOARD (5804)

A heavy "L" bracket on the board attaches to the chassis for heat sinking. This board provides voltages of +15 V, −15 V, +5 V, ÷14 V, and Vhd. Vhd is variable from 18 V to 24 V and must be calibrated to the specific multidot thermal printhead being used.

ECG BOARDS (5806 & 5807)

This set of two boards contains the isolated preamp and the ECG processing circuitry by which heartbeat event pulses are provided to the CPU Board for FHR calculation.

TIME/DATE SWITCH BOARD (5811)

This board, mounted to the foremost bottom section of the chassis, consists of three switches on the component side and a 4-pin header on the solder side.

DISPLAY BOARD (5812)

This board is mounted to the front panel and consists of a three-digit 7-segment display for indicating heart rate, a 2½-digit 7-segment display for indication of uterine activity, and a lightbar module for heartbeat indication. Also mounted on the board is the circuitry to drive the displays and seven operator control switches. A 26-pin header and a 6-pin header are mounted on the board's solder side.

CLAD BOARD (5814)

This board shields the analog preamps from the digital processor boards.

(Single Cardiotach)

MOTHERBOARD (5810)

This board holds the following boards: Multifunction (5800), Correlator (5801), CPU (5802), ECG (5806 and 5807), Recorder (5808, 5709, or 6808), and Clad (5814). It has 14 pc edge connectors (48 positions each) to accept 7 dual-edge connector boards. One row of 7 edge connectors is staggered to positively key the boards. Eight additional connectors allow connection to points outside the card cage.

CORRELATOR BOARD (5801)

This 8085A based board accepts an audio signal from ultrasound or phono circuitry and provides heartbeat event pulses to the CPU Board. AGC'd 80 Hz phono is sent to the Multifunction Board for squaring and audio output.

CPU BOARD (5802)

This 8085A based board accepts pushbutton, mode, heartbeat event, and UA digital signals. It calculates heart rate and uterine pressure and sends them along with mode, time/date, and other messages to the Recorder Board via a digital bus. The CPU Board also controls the displays.

RECORDER BOARD (5808 or 6709)

This 8085A based board accepts FHR and UA signals from the CPU Board and drives the multidot thermal printhead to form trending plots. Messages from the CPU and either the keypad (optional) or keyboard (optional) are formatted and also sent to the printhead. The Recorder Board also accepts input from the Mark pushbutton and controls the recorder stepper-motor.

(Dual Cardiotach)

MOTHERBOARD (5810)

This board holds the following boards: Multifunction (5800), ECG (5806 and 5807), Clad (5814), CPU (6802), Recorder (6665 or 6666), and Correlator (7180). It has 14 pc edge connectors (48 positions each) to accept 7 dual-edge connnector boards. One row of 7 edge connectors is staggered to positively key the boards. Eight additional connectors allow connection to points outside the card cage.

CORRELATOR BOARD (7180)

This is a Z-80 based board that accepts an audio signal from ultrasound or phono ciruitry and provides heartbeat event pulses to the CPU Board. After filtering and automatic gain control, phono signals are sent to the Multifunction Board for squaring and audio output.

CPU BOARD (6802)

This 8085A based board accepts pushbutton, mode, heartbeat event and UA digital signals. It calculates heart rate and uterine pressure and sends this information with mode, time/date, and other messages to the Recorder Board via a digital bus. Also, the CPU Board controls the displays.

RECORDER BOARD (6665 or 6666)

This 8085A based board accepts digital HR and UA signals from the CPU Board and drives the multidot thermal printhead to form trending plots. Messages from the CPU and either the keypad (optional) or keyboard (optional) are formatted and sent to the printhead. This board accepts input from the Mark pushbutton and controls the recorder stepper-motor.

4.2 COMMON BOARDS – THEORY OF OPERATION

4.2.1 MULTIFUNCTION BOARD (5800)

The circuitry on the Multifunction Board is divided into four major sections consisting of the Ultrasound Front End, Phono Front End, Pressure Processing, and the Audio Amplifier. A detailed discussion of each circuit follows.

ULTRASOUND FRONT END

The ultrasound transmit oscillator is formed by Q7 and 2.3-MHz crystal Y1. The frequency of the oscillator may be finely adjusted by capacitor C91. The oscillator is buffered by Q8 and Q9 and fed to the transmit crystal of the transducer through a tank circuit consisting of C79 and L10 which is adjusted for a 4 ± 0.1 V AC response at 2.3 MHz.

The ultrasonic sound waves emitted by the transmit crystal enter the maternal abdomen and create echoes when they encounter an interface between tissues of differing acoustic impedance. If the interface is moving either toward or away from the transducer, the frequency of the reflected sound differs from the frequency coming from the transducer. The receive crystals detect the reflected sound and convert it to an electrical signal. This signal is fed through a high-Q, 2.3-MHz tank circuit consisting of L6, C57, and R80 to the gate of FET amplifier Q5. The gain of this amplifier may be peaked at 2.3 MHz by adjusting L7 in the tank circuit it forms with C59.

The amplified signal is buffered by emitter-follower Q6 and fed to pin 1 of product detector A12 which multiplies it by the 2.3-MHz transmit oscillator connected at pin 8. This process converts the variations of the received frequency from 2.3 MHz caused by fetal heart movements to audio frequency variations at its output, pin 6. This output is filtered by A11 (pin 1), a bandpass filter with a low-frequency cutoff of 72 Hz, a high-frequency cutoff of 870 Hz, and a midband gain of 8.2; by A11 (pin 14), a high-pass filter with a cutoff frequency of 200 Hz and a gain of 17; then by A11 pin 8, a 2-pole Butterworth low-pass filter with a cutoff frequency of 600 Hz; and then by an additional bandpass filter A11 (pin 7) with a low-frequency cutoff of 48 Hz, a high-frequency cutoff of 660 Hz, and a midband gain of 36. This filtered signal is fed to the audio amplifier section of the board, and through connector pin 20 to the Correlator Board. The ultrasound front end is powered by a 12-V regulator, A10. Separate decoupling is provided for the transmitter and receiver amplifier sections by inductors L8 and L5. The 2.3-MHz transmit oscillator is divided to 36 kHz by U2 and fed to connector pin 21. It is used for various timing references on the CPU and ECG Boards and to provide a clock for the isolated power supply of the ECG 1 Board.

CAUTION: The unit **should never be turned on without the Multifunction Board** in place since the power supply may be damaged if not provided with clock signals.

PHONO FRONT END

The phonotransducer contains a low-noise preamplifier which is supplied with power of +15 V through connector pin 10. The preamplified signal enters at pin 11, passes through a high-Q 80-Hz bandpass filter, A4 (pin 7), and is fed to the Correlator Board for automatic gain control through pin 19. After this processing, it returns through pin 17 and passes through another identical 80-Hz bandpass filter, A4 (pin 8). The signal is then squared by multiplier A3, which doubles the frequency of the ringing caused by the bandpass filters to 160 Hz, and amplified by a factor of 3 by A4 (pin 14), before being fed to the audio amplifier section.

PRESSURE CHANNEL

The circuitry in the pressure-channel section performs the following five functions:

1. Converts the DC voltage from a strain gauge or todynamometer to a corresponding frequency for pressure computations by the supervisor CPU.
2. Detects if a strain gauge is plugged into the front-panel UA connector and produces the TTL-level DIRECT UA Enable.
3. Detects if a tocodynamometer is plugged into the front-panel UA connector and produces the TTL-level TOCO Enable.
4. Generates a +4-V reference for either a strain gauge or tocodynamometer bridge.
5. Generates a +10-V reference used by circuits on the 6802 Board.

The 4-V reference is applied to the pressure-transducer bridge excitation nodes. Pressure variations cause a differential voltage to appear across the remaining two nodes according to the formula:

$$V\ (\text{differential}) = SGF \times V\ (\text{ref}) \times \text{Pressure (mmHg)}$$

The constant, SGF, is the "Strain Gauge Factor" and depends on the transducer in use. The SGFs for Corometrics' transducers are as follows:

Strain Gauge = 5 μV/V/mmHg
Tocodynamometer = 4.16 μV/V/g

For a 4-V reference, the conversion factors become:

Strain Gauge = 20 μV/mmHg
Tocodynamometer = 16.67 μV/g

NOTE: Tocodynamometer measurements are only relative measures of uterine pressure. Strain gauge measurements are absolute measurements of intrauterine pressure in mmHg.

The differential voltage from either a strain gauge or tocotransducer is filtered (RF) and applied to a high-gain DC instrumentation amplifier consisting of A7 and A5. The nominal gain of the stage is 125.

After passing through summing amplifier, A9 (pins 5, 6, 7), the pressure signal is multiplied by an additional factor of 8 giving an overall gain of 1000. The summing amplifier also performs these functions:

1. Acts as a 3-Hz low-pass filter if a strain gauge is in use. (If a tocotransducer is being used, edge pin 15 is grounded causing pin 14 of A8 to go to −15 V. This turns on Q4, connecting C26 across C27 which lowers the cutoff frequency to 1 Hz to reduce the effect of respiration on the tocotransducer signal.)
2. Adds a −1-V offset (A9, pin 7) via R37 and the +4-V reference. (During the self-test routines, if a transducer is plugged into the UA connector, the supervisor CPU drives Edge Pin D high, turning on A8 (pins 6, 7, 8). This turns on Q3, inserting R38 which adds another −1-V offset. The effect is to add 50 mmHg to the pressure reading being currently printed on the strip chart.)

Amplified pressure signals and the −1-V offset are inverted in A9 (pins 1, 2, 3) and applied to the input of the V/F converter, A6. The A6 device restrictions limit the voltage at pin 2 to a range of 0 V to 15 V. Diodes D5 and D6 prevent negative voltage excursions and D7 limits positive voltages to less than 10 volts.

Pressure values are converted to frequency as indicated in TABLE 4-1.

PRESSURE READING	FREQUENCY CONVERSION	VOLTAGE READING (A6, pin 2)
−50 mmHg	0 kHz	0 V
+200 mmHg	16.32 kHz	+5 V

PRESSURE/FREQUENCY VALUES
TABLE 4-1

The converted pressure signal in kHz is sent to the supervisor CPU (5802 or 6802 Board) via Edge Pin C.

A6 also provides a +1-V reference at pin 4. This is applied to pin 10 of A9 where it is amplified to +4 V at TP4. The +4 V is set by means of R58. In turn, the +4 V is applied to A4 (pin 3) where it is amplified to +10 V for use on the CPU Board. Refer to DIAGRAM 11-3, Multifunction Board Block Diagram.

DIRECT UA Enable

A8 (pins 9, 10, 11) and A9 (pins 12, 13, 14) are used to determine if a strain gauge is plugged into the front-panel UA connector. A strain-gauge bridge that draws more than 4 mA from Edge Pin 17 causes the collector current in A8 to pull down the voltage at pin 12 of A9 below 15 volts. This drives A9 (pin 14) to −15 V which shuts off A8 (pins 3, 4, 5). This drives Edge Pin E high which represents the DIRECT UA enable.

TOCO Enable

When a tocotransducer grounds Edge Pin 15 and turns on Q4, it also shuts off A8 (pins 1, 2, and 3). This drives Edge Pin B high which produces the TOCO enable.

4.2.2 POWER SUPPLY BOARD (5804)

The power transformer mounted on the chassis has two primary windings with a number of taps which may be configured for various line voltages. It has four secondary windings. One goes directly to the chassis-mounted diode bridge and electrolytic capacitor. The voltage on the capacitor and the other three primary windings, each having a center tap, are connected to the 5804 Board through connector P20. Refer to **DIAGRAM 11-10.**

The first winding, entering at pins 5, 11, and 2, is full-wave rectified and filtered to provide an unregulated voltage of approximately +12 V to power the stepper-motor in the recorder.

The second winding, entering at pins 3, 7, and 6, also full-wave rectified and filtered, provides an unregulated voltage of about +9 V fed to regulator U2 to provide a +5-V supply adjustable by potentiometer R3.

The third winding, entering at pins 9, 1, and 12, is full-wave bridge rectified and filtered to provide complementary unregulated voltages of about +22 V. The positive unregulated voltage is brought out to power the audio amplifier. Both voltages are then regulated by U1 and U4 to provide +15 V and −15 V supplies.

The voltage from the chassis-mounted capacitor of about +28 V, enters at pins 10 and 4, and is regulated by U3 to a voltage which may be adjusted from +18 to +24 V by potentiometer R4.This voltage is used to power the printhead; the voltage adjustment is necessary because of the variation in resistance in the printhead elements.

If the +5-V supply fails, the circuitry consisting of D1, Q2, and Q3, shorts the adjustment pin of U3 to ground, reducing the printhead voltage to about +1.5 V. This is necessary since the printhead elements could be damaged if they are energized when there is not a +5-V supply to power the logic driving them.The printhead supply can be reduced to +1.5 V by application of a high logic level from the Recorder Board to transistor Q1.

All supply voltages are connected to the Motherboard via connector P21 (P12 on Motherboard).

4.2.3 ECG BOARDS (5806 & 5807)

The 115 ECG circuitry consists of an electrically isolated preamplifier for patient-connected electrodes and signal processing circuitry which detects the peak of the R-wave and sends heartbeat event pulses to the CPU Board. The following subsections discuss the ECG circuits in detail (refer to **DIAGRAM 11-9**). Listed below are the major ECG circuits:

- isolated preamp
- line frequency notch filter
- high and low pass filters
- level compressor
- AGC
- autopolarity

- fixed plus variable threshold
- peak detector
- rate discriminator

ISOLATED PREAMP POWER SUPPLY (5806)

T1 is driven by Q5 and Q6 at 36 kHz to supply power to the isolated patient-connected circuitry. Voltage produced at the secondary winding of T1 is rectified by D22-D25 and filtered by C76 and C77. Q13, Q14, and D21 provide regulated + 10 V, while Q15, Q16, and D20 provide regulated − 10 V to A14-A18.

ISOLATED PREAMP (5806)

ECG signals enter through Edge Fingers [$\overline{A}$] and [$\overline{B}$] to an instrumentation amplifier (A16, A17, and A18). The common-mode voltage is inverted by A14 and fed to the leg plate via [$\overline{X}$]. The driven leg plate helps to cancel the effect of common-mode patient voltages.

A15 reduces incoming line-frequency noise by driving the shield with the AC voltage appearing between isolated and non-isolated ground.

A17 drives Q17 with one thousand times the differential ECG input voltage. The current through Q17 is therefore proportional to the ECG input signal. This current is reflected in the primary of T1 and appears as a varying voltage drop across R103 and R104. A12 amplifies the AC signal and cancels the DC component by integrating the voltage at A12 (pin 7) and feeding the integral back via A12 (pin 1).

A13 is a 100-Hz low-pass filter. A13 (pin 6), also TP10, presents a band-limited and amplified (X1000) version of the differential ECG input voltage.

NOTCH FILTER (5806)

Two sections of A8 form a line-frequency notch filter. A portion of the signal at A8 (pin 1) is fed back via A8 (pin 7) to the twin-tee RC network (R64-R69, C45, C46, C50, and C51). The phase shifts in the network act to cancel frequency components at the line frequency.

HIGH-PASS FILTER (5806)

The remaining two sections of A8 form high-pass filters to reduce low-frequency noise and baseline roll.The signal at A8 (pin 14) has a low-frequency cutoff point of approximately 12 Hz.

COMPRESSOR (5806)

One section of A9 and D8-D13 forms a voltage compressor to allow a wider dynamic range of ECG amplitudes. Small amplitude signals have a gain of − 7.5 through this stage. Larger amplitude signals will forward bias some or all of the diodes (D8-D13), thereby lowering the feedback resistance and the stage gain.

LOW-PASS FILTER (5806)

Two sections of A9 form low-pass filters to reduce high-frequency noise. The signal at A9 (pin 8) has a high-frequency cutoff of approximately 80 Hz.

AGC MULTIPLIER (5806)

This stage sets the signal to the amplitude determined by the AGC control circuitry. A1 is a variable transconductance amplifier which provides a voltage gain from A9 (pin 8) to A10 (pin 1) which is a linear function of the current into A1 (pin 1); A1 (pin 1) approximates − 14 V. This current is proportional to the output voltage of the AGC integrator (TP4).

RANGE TRIM (5806)

R37 adjusts the circuit gain. This adjustment is required to ensure that specified upper and lower limits of ECG signal amplitudes will fall within the dynamic range of the system.

The 5806 Board also includes a DG212 quad analog switch (U2) which is used to optimize the gain and filtering of maternal QRS complexes.

If maternal ECG is being monitored, a jumper in the maternal ECG cable connector will pull Edge Finger ㉓ to ground. This will change the state of the switches in U2, thereby altering the gain and filtering.

When fetal heart rate is being monitored, Edge Finger ㉓ is high. R75 and R151 will then be shorted by U2 and the section of U2 in series with R157 will be an open circuit.

When maternal heart rate is being monitored, Edge Finger ㉓ is low. R75 is then placed in series with R59, and R151 is placed in series with R86. This reduces the high and low cutoff frequencies to maximize the signal-to-noise ratio for the maternal QRS complexes. R157 is placed in parallel with R51 which reduces gain by a factor of about 5. This gain reduction compensates for the fact that a maternal QRS complex is typically larger in amplitude than a fetal QRS complex.

AUTOPOLARITY (5806 & 5807)

The polarity of the ECG input signal can be either positive or negative, however the peak detector operation is based on a positive R-wave peak. The autopolarity circuit inverts the polarity of the signal, if necessary, to make the largest excursion of the signal positive at TP9.

D2, D3, C2, C3, and R8-R10 on 5806 sense the polarity of the signal at TP9. If the polarity is positive, the polarity control circuitry will be stable and 5806 Edge Finger Ⓢ (polarity correct) will be high. If the polarity is negative, 5806 Edge Finger Ⓢ will be low, enabling U7 on 5807. If the polarity remains negative for 8 seconds, U7 on 5807 will time out and toggle U3 on 5807. The new logic level appears on 5806 Ⓡ, changing the state of Q9 and making the R-wave positive at TP6.

30 HZ BANDPASS (5806)

The section of A11 feeding TP6 forms a passive 30-Hz bandpass filter to extract the maximum R-wave energy and to attenuate noise. The nominal peak at TP6 is approximately 4.5 V when the AGC is locked on the signal.

THRESHOLD (5806)

The 30-Hz filtered signal is inverted at A11 (pin 7) and fed to the threshold circuit. The threshold circuit inverts the signal and offsets it in the negative direction. This negative offset keeps the peak detector from triggering on noise since the peak detector responds only to positive signals. The offset has fixed and variable components. The fixed component is provided by R89. The variable component is derived from the AGC integrator (A2, pin 14) which is amplified by a factor of six at A3 (pin 7). For large ECG signals, A3 (pin 7) is at approximately 1.5 V and the threshold is at its minimum (about 50% of the 4.5 V R-wave). Progressively smaller ECG signals increase the threshold until it is at its maximum of 70% of the R-wave (A3, pin 7 at 14 V). The threshold is increased for small signals because they do not rise as far above the noise floor as large signals and a higher threshold gives more noise immunity.

PEAK DETECTOR (5806)

A11 (pins 12-14), D15, and C55 form a positive peak detector. When the output of the threshold circuit (A11, pin 8) rises above 0 V, A11 (pin 14) rises above 0 V, charging C55 to the voltage at A11 (pin 8) and forcing A4 (pin 13) high (new peak). After the crest of the R-wave, A11 (pin 12) falls below its previous value which is still present on A11 (pin 13) due to C55. A11 (pin 14) then goes negative, bringing A4 (pin 13) down to −15 V and starting the rate discriminator on the 5807 Board. If a larger peak appears before the rate discriminator times out (229 ms), C55 will charge to that value and A4 (pin 13), new peak, will again go high, resetting the rate discriminator until after the crest of the peak.

When the rate discriminator times out, it discharges C55 with a 200-µs pulse via 5806 Edge Pin Ⓝ, A4 (pin 14) and Q12. The peak detector is then reset. Just before the rate discriminator times out, it sends a 660 µs "peak detector inhibit" pulse to 5806 Ⓟ which forces A11 (pin 12) negative via A4 (pin 1). This inhibits the peak detector and prevents the possibility of producing a "new peak" signal due to noise between the time the 5807 Board produces a heartbeat event pulse and the time the rate discriminator resets itself.

RATE DISCRIMINATOR (5807)

Consisting of U5, U6, U9, and one section of U3, the rate discriminator prevents the production of successive heartbeat event pulses closer than 229 ms (226 BPM) and provides various timing signals for the AGC, peak detector, and the heartbeat event one-shot. After the rate discriminator has cycled and a heartbeat event pulse has been produced, but before the 5806 peak detector has detected a new peak, 5807, U3 (pin 13) is high. This keeps U6 reset.

When the peak detector detects a signal greater than threshold, ㉔ on 5807 (new peak) goes high. This sets U3 (pin 13) low but U6 remains reset until after the crest of the peak, when "new peak" goes low. When "new peak" goes low, U6 begins counting. If the peak detector senses a peak greater than the previous peak, "new peak" will go high once again and reset U6. U6 will begin counting when the new peak has passed. If "new peak" stays low for 228 ms, 5807 ⑬ goes high to inhibit the peak detector. 400 µs later, 5807 ⑫ goes high to reset the peak detector capacitor, triggers the heartbeat event pulse one-shot (5807, U2, pin 13), and provides a timing signal to the 5807 AGC circuitry. Approximately 200 µs later, U5 (pin 4) goes high, setting U3 (pin 13) high, thereby resetting U6. U6 is then held reset and its outputs, and the outputs from U5, are all low. The circuitry is stable in this state until the 5806 peak detector produces another "NEW PEAK" pulse.

EVENT PULSE (5807)

The section of U2 feeding Edge Finger Ⓨ is configured as a one-shot. Its purpose is to stretch the pulse from U5 (pin 7) (see Rate Discriminator) long enough for the CPU Board to respond to it. The event pulse at Ⓨ can vary from 2.8 ms to 15 ms, depending on component tolerances.

AGC CONTROL (5806 & 5807)

The AGC basically consists of a multiplier in the signal path (see AGC Multiplier), an error amplifier (A2, pin 8) and an integrator (A2, pin 14). The integrator drives a current source (Q4) which in turn drives the control input of the multiplier, thereby adjusting the system gain. If the signal is at the proper level (4.5-V peak at TP6), the output of the error amplifier (TP3) is 0 V and the integrator output (TP4) is stable. If the signal is not at the correct level, TP3 will have a non-zero voltage which will drive the integrator output to the level that adjusts the gain of A1 (pin 5) to obtain the correct signal level.

D1 and C1 peak detect the 30-Hz fetal signal. When a heartbeat event pulse is produced by the rate discriminator, two sequential 890 µs pulses are produced by the 5807 Board. The first pulse drives 5806 Ⓚ high, which turns on Q1 via A5 (pin 1), thereby transferring the peak voltage on C1 to C5. The second pulse drives 5806 Ⓜ high which discharges C1 by turning on Q2 via A5 (pin 7). If no event pulses occur for 2 seconds, U1 (pin 3) on the 5807 Board will go high, allowing the production of the sequential pulses at 5806 Ⓚ and Ⓜ.

The voltage on C5 feeds an error amplifier A2 (pin 8). The error amplifier output feeds the integrator A2 (pin 14) through a multiplier A1 (pin 12). Both sections of the multiplier (A1) have a gain proportional to the integrator output since the integrator drives Q4 which provides control currents to the multipliers. Thus, for a given error signal, the rate of change of voltage at the integrator output will be proportional to the voltage. This arrangement allows the rate of change of gain to be proportional to the gain, thereby eliminating excess "hunting" at high signal amplitudes.

The integrator output is constrained from going below 0.26 V by one section of A3 (pin 1), thus setting a limit on the minimum multiplier gain.

Two sections of A6 on 5806 work together with U4 on 5807 and Q3 on 5806 to prevent short noise bursts in the signal from upsetting the AGC level. The resistive divider consisting of R33-R35 sets A6 (pin 2) to 5.6 V and A6 (pin 5) to 2.5 V. Normally the voltage on C5 will be 4 V. A6 (pin 1) will then be at -12 V, keeping Q3 from conducting. A6 (pin 7) is normally high. If there is enough noise on the signal to drive the voltage on C5 greater than 5.6 V, A6 (pin 1) will go high allowing

Q3 to clamp the integrator input voltage to 0 V, thereby freezing the AGC. When A6 (pin 1) goes high, it also triggers U4 on 5807 via 5806 Edge Finger Ⓕ. U4 is a one-shot with a 2.2 second output pulse. C9 charges through R9 to 2.5 V in 3.3 seconds. If 2.5 V is reached, A6 (pin 7) on 5806 goes low, shutting off Q3 and allowing the integrator to respond to the error signal.

TIME BASE/ECG TEST SIGNAL (5807)

U8 is a counter which provides 1-Hz, 2-Hz, and 4-Hz square waves for timing of various circuits. The ECG test signal is derived from the 2-Hz square wave at U8 (pin 11). R18 feeds a 121-ohm resistor on the ECG leg-plate tester, the other side of which returns to ECG for testing. The test signal is not intended to have a waveshape simulating a fetal QRS complex. D1, C17, and the associated resistors form a fast-charge/slow-discharge circuit. When the leg plate is connected to the leg-plate tester, the filtering on the 5806 Board will attenuate the discharge phase more than the charge phase, thereby allowing the autopolarity circuit to select the charge phase to be positive. R18 and the 121-ohm resistor on the leg-plate tester form a voltage divider which attenuates the test signal to a level simulating a fetal QRS wave of roughly 500 μV peak.

4.2.4 DISPLAY/SWITCH BOARD (5812C)

This board, mounted on the front bezel, holds seven switches, a lightbar module, six numeric displays and their associated components. P4 provides the interface with the CPU Board and P5 connects to the "Record" and "Power ON" LED's. The "heartbeat" lightbar (DS4) illuminates when P4 (pin 15) is low.

DS1, DS2, and DS3, form the multiplexed 3-digit heart rate display. U1 converts the BCD data from the CPU Board (BCD1-BCD4) to a 7-segment code (a-g).XFER1, XFER2, and XFER3, enable DS1, DS2, and DS3, respectively, when high.

DS5, DS6, and DS7, form the multiplexed 3-digit Uterine Activity Display. U3 latches the uterine activity data present on BCD1-BCD4 on the rising edge of DISPL STRB at P4-17. U2 converts the latched data to a standard 7-segment code for DS6 and DS7. XFER1, XFER2, and XFER3, enable DS5, DS6, and DS7, respectively, when high.

DS5 is a "Universal Overflow" display, capable of displaying the following figures when the corresponding segment bits (denoted by the letters "abcde" on DS5) are low:

1	−	÷	÷1	−1
ab	c	cde	abcde	abc

DS5 is wired to the 7-segment bus differently than DS6 and DS7 (which are ordinary "Decimal" displays). This permits the use of a single decoder (U2) which illuminates the corresponding figure indicated in truth table, TABLE 4-2.

FIGURE	ABCD	a	b	c	d	e	f	g
1	0111	0	0	0	1	1	1	1
÷1	1000	0	0	0	0	0	0	0
−1	1001	0	0	0	1	1	0	0
−	1100	1	0	1	1	1	0	0
÷	1010	1	1	1	0	0	1	0
Blank	1111	1	1	1	1	1	1	1
DS5 BITS →		a		b	d	c		g

U2 BITS — SINGLE DECODER
TABLE 4-2

4.3 SINGLE-CARDIOTACH BOARDS — THEORY OF OPERATION

4.3.1 CORRELATOR BOARD (5801)

The Correlator Board's circuits accept either unprocessed phono or ultrasound audio signals and produce heart-rate event triggers which are routed to the Supervisor CPU (5802 Board) for HR computation. Autocorrelation is a dynamic technique which senses periodicity in a complex waveform by comparing a current time slice of the waveform with a time slice from the past of the waveform. If the similarity is acceptable, an event pulse will be generated. On the other hand, if the waveforms don't match very well, the correlator will wait until a better match is found. The technique is a dynamic one since if a sufficiently long period with no acceptable match occurs, the correlator will replace the old time slice with a current one to be used as a reference. In this way, the correlator adapts to changing clinical environmental parameters such as a change in fetal heart rate, or fetal or maternal movement that changes the character of the waveform.

In essence, the autocorrelation processing is performed by dedicated microprocessor-controlled hardware with the majority of functions controlled by the resident program in the 2764 PROM (U5). To check the operation of this subsystem, refer to the Correlator Self-Test in Section 6 (TROUBLESHOOTING). However, in addition to the digital hardware which performs the actual processing there is an analog section which interfaces either the phono or ultrasound signals with the digital correlator hardware.

ANALOG SECTION

Ultrasound or phono signal selection is determined by the logic level of Edge Pin ⑧. A high drives comparator A2 (pin 7) to +15 V which turns on switch Q3. This routes the ultrasound signal from Edge Pin Ⓨ to the input of AGC-controlled amplifier Q4 (pin 3). The AGC signal at Q4 (pin 2) can vary the gain from −60 dB to +20 dB. (See 5801 schematic diagram.)

A similar process takes place if Edge Pin ⑧ is low; only phono signals are routed to Q4 via Edge Pin Ⓩ. The phono or ultrasound channels are almost identical except that the ultrasound channel has an insertion loss of 20 dB (R38 and R39) while the phono channel has a gain of 5 dB at A2 (pin 8).

The AGC loop consists of A2 (pin 14), A4 (pin 8), A4 (pin 10), and A1 (pin 7). The first stage (A2, pin 14) provides an additional 22 dB of gain. The output is also routed to Edge Pin Ⓐ which serves as the input for the audio chain used with either the rear-panel speaker or the headset.

If the audio level at A4 (pin 6) is less than 0.7 V (the base-to-emitter drop), A4 is nonconducting and the quiescent voltage across C38 will be determined by clamp A4 (pin 1). However, if the voltage at A4 (pin 6) exceeds 0.7 V, A4 (pin 8) conducts and the voltage across C38 increases which injects current into the base of A4 (pin 9). This applies an increasing positive voltage to A1 (pin 5). The resulting voltage is level-shifted, scaled, and then applied to gate 2 of Q4. The AGC voltage (TP10) should range from −4 V (minimum gain) to +2.5 V (maximum gain).

The AGC-controlled voltage is applied to half-wave active rectifier A1(pin 8), and from there to 60dB-inverting amplifier A1 (pin 13). This is followed by a 2-pole, 10-Hz Bessel filter A1 (pins 1, 2) which creates the envelope for the A/D converter.

The envelope is then integrated and buffered by A3 (pin 1). Then A3 (pins 6, 7) inverts the signal and adds an appropriate offset. This voltage serves as the A/D converter reference and should be in the range from -15 to -6 V at TP12. Also, note that the reference (TP12) is also summed at A1 (pin 13). This provides a negative shift in the baseline for high signal levels.

The gain-controlled reference is necessary in order to prevent an accumulator overflow from an A/D conversion value outside of the range of the correlator. (This could occur on noise peaks or other signals of excessive amplitude.)

DIGITAL SECTION

The digital hardware can be broken down into three subsections:

- 8-bit Microprocessor: This subsection can be further broken down into the 8085A microprocessor (U1), 8-K PROM (U5), 1-K static RAM (U9 and U10), and the RAM, I/O port, and timer chip (U11).
- A/D Converter: The A/D converter is U3.
- Multiplier/Accumulator: The 8-bit by 8-bit accumulator/multiplier is U13.

As noted previously, the autocorrelation processing is controlled by the firmware in PROM, U5. Other PROM modules contain routines affecting hardware which perform the following functions:

1. Initialize the timer in U11 to provide a pulse train with a period of 2.5 ms to drive the RST 7.5 interrupt.
2. Acquire and store waveform samples from the A/D converter.
3. Determine the operating mode (US or Phono).
4. Toggle PC4 (pin 2) of U11 to signal a heart rate event to the Supervisor CPU via Edge Pin [F].
5. Use U13 to multiply two 8-bit numbers and add the product to a number in the U13 19-bit accumulator.
6. Clear the multiplier and/or accumulator since the device has no master reset or clear line.
7. Initiate self-test procedures which check the microprocessor, RAM, ROM (CRC test), U11 RAM, and U13 when TP3 is jumpered to TP1. (LED DS1 remains on during the test and flashes at the end if all tests pass.) In event of a failure, the source may be located by examining the output of a DAC test board plugged into the edge connector located on the top of the 5801 Board. (The microprocessor controls the DAC via the address at 6001 hexidecimal.)
8. Initiate the ramp test if TP4 is jumpered to TP1. This routine essentially tests the interface between the Correlator and the Supervisor (5802 Board) microprocessors. (LED DS1 goes on at the start of the test and indicates the end when it flashes.)

NOTE: These are the only diagnostic tests for the autocorrelator. Self-test routines initiated by the front-panel Test push-button do not include tests for this subsystem.

Bus Management, Chip Enables, and I/O Port Clocks

The "Address Latch Enable" (ALE), pin 30 of U1 goes high when the address bus changes state and goes low when the lines are stable. The trailing edge is used to strobe the low-order address bits onto the A0-A7 address lines via U4 (pin 6) and latch, U12.

The ALE line is also used to implement a look-ahead decoder consisting of U6, U7, and their associated gates. On the trailing edge of the ALE pulse, the decoded addresses appear at U27 (pins 4, 7, 9, 10, 12). Since a read or write strobe doesn't appear until approximately 200 μs later, the enabled devices have sufficient time to settle. U4 (pin 3) clears pin 6 of U6 when a read or write pulse occurs and the decoder is disabled until the next ALE pulse.) A15 is also used as a "fast" enable for RAM I/O Timer, U11.

The A/D conversion is controlled by RST 7.5 interrupt-driven routines which occur every 2.5 ms. A/D data is strobed onto the data bus by addressing 6002H (hexadecimal) which enables pin 15 of U3. (This action also initiates a new conversion cycle whose result is read on the next RST 7.5 interrupt.) Once the data is read by the microprocessor, it is stored in the appropriate data file in U9 or U10.

The correlation processing requires the multiplication of two 8-bit numbers and the resulting product is then added to a stored sum. Although the routine could conceivably be implemented in software, because of the time constraints involved, it is practically implemented in hardware via the TRW 1008J multiplier.

There are 7 control lines of interest, 16 input lines, and 19 output lines. The data to be multiplied is applied to the X input (pins 22-29) and the Y input lines (pins 32-40) of U13. The control lines TSL, TSM, and TSX are set and the PREL line is cleared through the PC ports of U11. This puts U13 in the data-input mode. To form the product, the microprocessor executes a "Load A" instruction at 6000H which generates a positive-going pulse at CLK Y AND CLK X (pins 31 and 32 of U13). The product is then added to the accumulator by a "Load A" instruction at 6003H. This generates a positive-going pulse at CLK P (U13, pin 7).

Since the product or accumulator ports of U13 can be tri-stated or enabled, it is possible to interface the data inputs and the accumulator outputs through the same ports. For this reason, the A and B ports of the 8156 (U11) are used for both input and output.

To read the sum in the accumulator, the PREL line is cleared. The TSX, TSM, and TSL lines are set or cleared to strobe the P0-P18 lines of U13 on the PA and PB Ports of U11 in a sequence determined by the microprocessor.

4.3.2 CPU BOARD (5802)

The CPU Board is the supervisor of the monitor. It accepts inputs from switches, mode inputs, heartbeat event pulses, and a frequency input from the pressure channel. It calculates heart rate and uterine pressure. It sends heart rate and uterine activity data to the Display Board and the Recorder Board. In addition, it sends time/date and message codes to the recorder.

The processor is an 8085 running at 6 MHz. A 2764 8K PROM holds the program. 256 bytes of static RAM reside in an 8155 and 50 bytes of battery-backed RAM reside in U27. Device-select pulses are generated by a pair of 74F138 3-to-8 decoders (U8 and U9).

The I/O ports on two 8255s and one 8155 provide most of the I/O to and from the edge fingers. An MDAC and an op-amp (U13 and U14) control the audio volume.

A battery backed real-time clock chip (U27) provides time and date to the processor.

TIME BASE

U10 sends the 6 MHz clock to the 8085 and to the Recorder Board via 18. U1-U3 supply time bases to the ECG Boards and the Recorder Board as well as driving the 8085 RST 7.5 pin at 1.123 kHz. The 8085 uses this signal as a time base for processing.

Device-Select Logic

The device-select pulses are generated by a pair of 3-to-8 decoders, U8 and U9. U8 selects I/O devices and U9 selects memory devices. The conditions required for selection of each device are shown in TABLE 4-3.

IO/M	A14	A13	A12	DEVICE SELECT NAME	DEVICE SELECTED
0	0	0	X	$\overline{Y0M}$	U12 (PROM)
0	0	1	X	$\overline{Y1M}$*	U27 (CLOCK CHIP)
0	1	0	X	$\overline{MP1}$	U22 (RAM)
1	0	0	0	$\overline{MP1}$	U22 (I/O or TIMER)
1	0	0	1	$\overline{Y1P}$	U7 (I/O)
1	0	1	0	$\overline{Y2P}$	U23 (I/O)
1	0	1	1	$\overline{Y3P}$	U14 (AUDIO DAC)

*Y1M High true at U5 (pin 2)

CPU DEVICE SELECTION
TABLE 4-3

ADDRESS LATCH AND PROM

Unlike all other bus-connected devices on the CPU Board, the PROM (U12) does not contain address latches to demultiplex the address/data lines, AD0-AD7. U11 latches AD0-AD7 lines at the falling edge of ALE. A0-A7 and A8-A12 address any of the 8K bytes in PROM.

CLOCK/CALENDAR

U27 is a battery-backed clock/calendar chip which also contains 50 bytes of battery-backed RAM. The 4-V battery is located in the chassis, not on the board. The 32.768 kHz time base for the clock is generated by U26, Y2, and associated components.

When the monitor is off, U26 and U27 are powered by the battery through D1 and Q2. When the monitor is on, the battery is charged by D3 and R63.

Pin 22 of U27 is a power-sense pin. If the battery becomes discharged to the point where U27 (pin 22) is less than +3 V, the operation of U27 is not guaranteed. U27 (pin 22) senses this and clears a flag. The flag remains cleared in spite of any further changes in power and can be set only by the 8085. During the initialization routine, the 8085 interrogates the power-sense bit. If the bit has been cleared, the CPU Board sends a code to the Recorder Board to print the message "SET TIME/DATE" on the chart paper. This message is repeated until the CPU Board senses the "Time/Date Set Enable" switch going active.

U5 is required for reliable operation of U27. U5 is a transparent latch which conditions the chip enable for U27 by blocking it until the rising edge of ALE. Q3 ensures that no battery current is drained by chip-enable circuitry when the monitor is off. The time and date are set as described in the operator's manual. The signals applied to the CPU Board from the Time/Date setting switches are shown in TABLE 4-4.

CPU EDGE FINGER	NAME	PORT
Ⓑ	$\overline{\text{TD ENABLE}}$	U23 PA7
R	$\overline{\text{TD SEL}}$	U23 PC7
13	$\overline{\text{TD}}\downarrow$	U23 PC6
P	$\overline{\text{TD}}\uparrow$	U23 PC5

TIME/DATE SETTING SWITCH SIGNALS
TABLE 4-4

INITIALIZATION AND POWER-ON RESET

A shunt regulator (D4) along with Q4 and associated resistors form part of a reset circuit. When the 5-V supply line is less than approximately 4.7 V, D4 does not conduct and Q4 is off. U27 is held reset by R65 and R66, U27 chip-enable is inhibited since Q5 is off, and the 8085 is held reset since there is no voltage on C51. The 8085, in turn, keeps other devices reset via its reset output (U15, pin 3). When the 5-V supply line exceeds 4.7 V, D4 conducts which takes U27 out of reset and allows C51 to begin charging through D5 and R80. When C51 charges to logic 1 (approximately 30 ms), the 8085 is no longer held reset and its reset output goes low. Approximately 5 μs later Q6 turns off, turning on Q5, thereby stopping the inhibit on U27 chip-enable. During power-down, when Q4 shuts off, Q9 turns on which discharges C51 rapidly. R95 provides hysteresis in the power-up circuit.

Q6 is required since the state of U5 is indeterminate between the time power is applied to the board and the time U5 receives the first ALE pulse. When the 8085 comes out of reset, it addresses PROM at address 00. The ALE pulse produced will initialize U5 (pin 2) to logic 0. A few microseconds later, Q6 shuts off, enabling the chip-enable circuitry for U27.

HEART RATE RELATED SIGNALS

The transducer assemblies and leg-plate assembly contain jumpers which pull the mode-select lines down to 0 V when the transducers are connected. Thus, when the ultrasound (US) transducer is used, CPU Edge Finger Y is low. Similarly, when the phono transducer is used Z is low. If the ECG leg plate is connected, 21 is low.

The 8085 polls U23 PC0 (ECG), PC1 (US) and PC2 (Phono) to determine which mode has been selected. U20 inhibits the phono and US mode-select signals if either of those transducers is connected while the leg plate is connected. Thus, ECG mode always predominates in the event of ambiguous mode signals. U18 and U19 select incoming heartbeat event pulses that correspond to the selected mode and route them to the 8085 RST 6.5 interrupt input. DS2 aids in troubleshooting by flashing at each incoming heartbeat event pulse. If no transducers are connected, Ⓢ (HR INOP) will be high. The 8085 measures the interval between heartbeat event pulses and calculates the heart rate. Heart rate is sent to the Recorder Board via U7 Port A and to the central station via U22 (Port A), U25 and U28. Four-beat averaged heart rate is sent to the Display Board via U7 (Port B).

For every "valid" heartbeat, Edge Finger 19 goes low for approximately 100 ms, thereby flashing the heartbeat LED on the Display Board. This signal is also available at J102 (via CPU Edge Finger Ⓣ) for use by an external data acquisition system. The ±1.2 V HR signal (at V and J102, pin 7) can be strobed into the data acquisition system on the rising edge of "XFER ↑" (at Ⓣ and J102, pin 13).

In ECG mode, Finger [2] will pulse high for approximately 100 ms for every heartbeat event pulse. This causes the audio section of the Multifunction Board to produce a beep in the speaker.

When any two successive heart rates differ more than 25 BPM, Finger Ⓧ (Penlift 2) goes high and the Recorder Board is sent a message to interrupt the heart rate trace. Penlift 2 is available on J102 (pin 15) for use by a remote alert system. "Penlift Out" at finger ㉑ acts as Penlift 2 does, but is an open collector output to drive the pen solenoid on a remote recorder. "Penlift Out" is available at J102 (pin 8). In ECG mode, if the "ECG Artifact Elimination" switch is set to "OFF" (CPU Finger Ⓨ high), there will be no penlift signals.

The ± 1.2 V HR signal at Finger [V] is derived from U22 (Port A), which feeds a DAC (U25). The output current from the DAC is changed into a voltage by one section of U28. The scaling is listed in TABLE 4-5.

HEART RATE	U22 PORT A	VOLTAGE AT [V]
0 bpm	0	−1.2 V
120 bpm	120	0 V
240 bpm	240	+1.2 V

HEART RATE MODE OUTPUT VOLTAGES
TABLE 4-5

UTERINE ACTIVITY RELATED SIGNALS

The mode inputs, "Direct UA" at Finger [A] and "Toco" at [F] come from the Multifunction Board. The Multifunction Board pressure section feeds CPU Finger Ⓖ with a frequency in the range of 0 - 16.32 kHz. A change in frequency of 65.28 Hz represents a 100 mmHg change in uterine pressure (or a change of 100 on the 0 - 100 Toco scale). The frequency is applied to U22 (pin 3) which clocks the timer in U22. By reading and re- initializing the time at approximately an 8-Hz sampling rate, the 8085 derives the pressure value. The pressure value that is derived is relative to the value that was present when the Pressure Zero button was last pressed. (The front-panel Pressure Zero button brings CPU Finger [12] low when it is activated.) The incoming frequency range that can be "zeroed" by the Pressure Zero button is from 0 to 9792 Hz. A typical frequency in "direct" mode at 0 pressure is 3264 Hz.

The ± 1.2-V pressure signal at Finger [W] is derived from U22, Port B, which feeds a DAC (U24). The output current from the DAC is changed into a voltage by one section of U28. The scaling is found in TABLE 4-6.

PRESSURE	U22, PORT B	VOLTAGE AT [W]
0 mmHg	0	−1.2 V
50 mmHg	50	0 V
100 mmHg	100	+1.2 V

UA MODE OUTPUT VOLTAGES
TABLE 4-6

NUMERIC DISPLAY INTERFACE

The 6-digit multiplexed numeric readout (3 for ECG and 3 for uterine activity) is driven by 8 signals from the CPU Board. Refresh rate is approximately 375 Hz. BCD oncoded numeric data is transmitted on BCD1 - BCD4 (PB-PB). The digit strobes (XFER-XFER3) are produced by U7 PB5-PB7 and buffered by U4. Blank (U7 PB4) is asserted during digit strobe transitions and whenever the display is blanked.

RECORDER RELATED

U7 is used to send message codes and trending data to the Recorder Board. The Recorder Board drives the multidot thermal printhead which plots trending curves and prints messages on the chart paper. REC b_0 - REC b_7 send data while REC OBF and SUP ACK provide handshaking. When the CPU Board has a data word to send to the Recorder Board, CPU Finger Ⓢ (REC OBF) goes low. When the Recorder Board has accepted the data, it brings CPU Edge Finger ⑯ (SUP ACK) low. After the cycle is complete, CPU Fingers Ⓢ and ⑯ are both high.

If the Recorder Board does not respond to REC OBF with SUP ACK within a reasonable time, the CPU Board assumes that the Recorder Board has malfunctioned and traps it by bringing Finger Ⓤ (REC TRAP) high (see U22, pin 39).

The message codes are given in the Recorder Board (5808 or 6709) Theory of Operation. Miscellaneous recorder-related signals are listed in TABLE 4-7.

CPU EDGE FINGER	NAME	DESCRIPTION
[11]	RECORD	Senses front-panel Record button activation. The Recorder Board is sent the ON or OFF message via U7 (Port A).
[X]	RECORD LED	Activates the front-panel record LED.
⑰	SUP PAPER LOW	From Recorder Board. Causes the record LED to flash (if the recorder is ON).
⑲	SUP PAPER OUT	From the Recorder Board. Causes the CPU Board to latch the recorder status to OFF.
Ⓣ	PAPER ADV	From the Display/SW Board. Causes recorder to advance paper at 25 cm/min. Twenty seconds after a low-to-high transition, the CPU sends the following information to the recorder via U7 (Port A): Mode Information Time and Date Chart Speed
Ⓕ	SUP READY TO REC	From the Recorder Board. It goes low during recorder self-test. A low-to-high transition signals the CPU Board that the recorder test is complete. The CPU Board will trap the Recorder Board via CPU Finger Ⓤ if for any reason Ⓕ stays low for an unreasonably long period of time.
[9]	SPEED OVERRIDE	From rear-panel connector J102. If this line is held low for at least 120 ms and then brought high, the CPU will send a mesage to the recorder Board (via U7, Port A) to run the recorder stepper-motor at its highest trending speed.

RECORDER RELATED SIGNALS
TABLE 4-7

ELECTRONIC VOLUME CONTROL

The audio volume of the monitor is controlled by U14, an 8085 compatible MDAC with internal data latches. The 8085 sends a data word from 0 (volume off) to 255 (maximum volume, no attenuation) to the DAC in response to the front-panel volume control pushbuttons. Holding the "Volume Up" pushbutton down (Finger [14] low) decreases the attenuation from Finger ⑬ to ㉔ whereas the "Volume Down" pushbutton (Finger [S] low, when activated) increases the attenuation.

WATCHDOG TIMER

U6 is a counter which monitors operation of the microprocessor and restarts it in the event of a malfunction (i.e.due to static discharge).

U6 is clocked by an 8-Hz square wave at pin 1. Normally, the processor will continuously send reset pulses (repetition rate > 2 Hz) to U6 (pin 2) via U7 (pin 22), C42, and R16. These pulses reset U6 before U6 (pin 9) has a chance to go high. Since U6 (pin 9) is normally low, Q11 is off and the watchdog timer circuit has no effect.

If the processor malfunctions, it will not be able to send reset pulses to U6. In 500 ms U6 (pin 9) will go high, turning on Q11 which will turn off D4 and Q4, thereby allowing C51 to be discharged by Q9. U15 (pin 36), reset in, will then go low which will reset the processor (U15). When the processor is reset, U15 (pin 3) goes high, thereby resetting U6 via R96 and R16. U6 (pin 9) then goes low allowing U15 to come out of reset and begin program execution from the power-up condition.

TELEMETRY

If the **Model 320 Telemetry** unit is properly connected to the 115 Fetal Monitor, and is powered, the CPU Board will send the code to the Recorder Board to print the word "TELEMETRY" on the chart paper. This code will only be sent if the following conditions are met:

1. Telemetry at CPU Finger ⑦ is low.
2. ECG at CPU Finger [21] is low.
3. Toco at CPU Finger Ⓕ is high.

4.3.3 RECORDER BOARD (5808 or 6709)

NOTE: Refer to Section 10.1 for the RS-232C Serial Interface Guide for the 6808 Recorder Board. Refer to Sections 10.2 through 10.4 for the Theory of Operation, including RS-232C and COROLAN Interface Guides, for the 7383A and 7383B Recorder Boards.

The Recorder Board plugs into the card cage Motherboard. Three plugs on the board provide the following interfaces:

1. P17: This plug accepts the connector for the optional 2115 Keypad or 2116 Keyboard.
2. P18: This plug accepts the connector for the recorder stepper-motor.
3. P19: This plug accepts the connector for circuits performing the following six functions:
    - Thermal printhead element power.
    - Printhead serial-in/parallel-out shift registers and controls (DOT CLK, DOT DATA, and LOAD).
    - Printhead enable strobes (STB0-STB4).
    - Power for "Paper Low" and "Paper Out" optosensors (OPTO DRIVE A and OPTO DRIVE B).
    - Optosensor outputs for PAPER LOW and PAPER OUT.
    - Printhead electronics power (+5 V).

HARDWARE/SOFTWARE

Hardware and software on the Recorder Board perform the following functions:

1. Accept message pointers, HR data, and UA data from the supervisor CPU Board for printing on the strip chart.
2. Accept message pointers and patient data entered from the optional 2115 Keypad or 2116 Keyboard.
3. The recorder processor builds the message string (and any data string) and determines the line where the string(s) will be printed. The software also computes the graphics dot position from the HR and UA data.
4. Step the recorder chart-paper motor, load alphanumerics and graphics dot patterns into the printhead, and fire the dot elements in the printhead.

Microprocessor

The microprocessor (U4) is an 8085 timed by the 6-MHz clock on the main CPU Board. The LSBs of the address bus (A0-A7) are strobed and latched into U22. Combined with A8-A12, these lines form the 13-bit address bus permitting access to blocks of memory with a maximum of 8-K storage.

The 3 high-order bits (A13-A15) select the memory or I/O peripheral to be accessed (partial decoding) via U13 and U14. Memory consists of 2K of RAM (U6) and 8K of ROM (U7). I/O peripheral devices include the 8155 RAM I/O timer (U5) used as an I/O port and 7.7-RST interrupt timer. U21 is an 8-bit input port which accepts message pointers and data relating to messages, HR, and UA sent from the supervisor CPU. U5 and U20 are used to manage handshaking signals with the CPUs of the Supervisor and optional Keypad or Keyboard.

STEPPER-MOTOR/PRINTHEAD INTERFACING

The following subsections address the Recorder Board circuitry that is associated with control of the stepper-motor and printhead.

Printhead Protection Circuits

A thermal process is used to generate the dot pattern which makes up the graphics and alphanumerics on the strip-chart paper. Each dot is formed by one thin-film resistor element in a linear array of 512 elements across the printhead face. Because of the array density and the power required for each element, the maximum time an element can be energized is approximately 7 ms. To ensure this time is not exceeded, both hardware and software measures are employed. The schematic diagram of the printhead is shown in FIGURE 4-1. The elements are represented by the line of resistors, R1-R512. Note that the supply bus (Vhd) to each element is switched by a series transistor controlled by an AND gate. The gate can only be enabled by one of the four strobe lines, STB0-STB4. In turn, strobe lines are enabled or locked-up high by hardware on the Recorder Board.

Power-Up Sequence

When power is first applied to the monitor, R1 and C1 hold pin 6 of U1 low for approximately 100 ms. At power-up, the supervisor processor produces a RESET OUT signal to the recorder CPU at U4 which tri-states its address bus. Pull-up resistors RN2 pull the bus high which ensures a high at U13 (pin 15) regardless of the states of its enable lines during at least part of the 100-ms period when pin 6 of U1 is held low. This sets the U1 flip-flop (pin 3) low, which disables the strobe lines until the first I/O write to address 0xH or 1xH (x = don't care, H = hexadecimal).

Once the recorder CPU has been reset, it can clear the printhead shift registers and the printhead gate-enable latches with an LD pulse. (This action prevents the writing of a random string of dots on the strip chart when the recorder is activated.) When the recorder CPU is not printing data on the strip chart, U2 (pin 2) is low which holds counter U11 reset. When the CPU fires the printhead elements, and the strobe line goes low, U11 begins counting. If the strobe lines remain low in excess of 7 ms, Q6 of U11 goes high which disables the counter clock and drives the head shut line high also. This action shuts down the printhead power supply which prevents any possible damage to the thermal elements.

In a properly operating system, a head shutdown occurs if any of the strobe lines (TP5) are grounded for more than 7 ms. However, note the following precaution.

CAUTION: Be careful to avoid grounding the strobe lines (TP5) in the event of a recorder malfunction since U11 will not trigger a head shutdown if the IC is defective or if it is not receiving a 9-kHz clock pulse.

Paper-Out/Paper-Low Alerts

A paper-out condition will also initiate a head shutdown and it will alert the recorder CPU via I/O Port PB7 (U5, pin 34). The recorder CPU will shut off the stepper-motor and signal the supervisor CPU via SUP PAPER OUT (U5, pin 1 →H) of the condition. The supervisor CPU will shut off the front-panel "Record" LED and will not respond if an attempt is made to activate the recorder by depressing the Record pushbutton. Once the PAPER LOW optosensor encounters the black squares on the strip chart, it cuts off and pin 10 of U18 goes high. This drives the output of the comparator (pin 13) low, which controls I/O Port PB6 (U15, pin 35). This allows a software counter to increment by 3 for each time the motor stepping routine

runs. If "white" is detected, the counter is decremented by 1. This suppresses a false PAPER-LOW alert (such as might be caused by a small imperfection on the paper) while initiating a PAPER-LOW alert when the paper advances approximately halfway through the first black square.

PRINTHEAD MODES

Dot data must be presented to the thermal element gates for each slice of chart paper; a "slice" being one step of the recorder chart-drive motor. Data is printed via the slices in one of three modes:

Graphics Mode

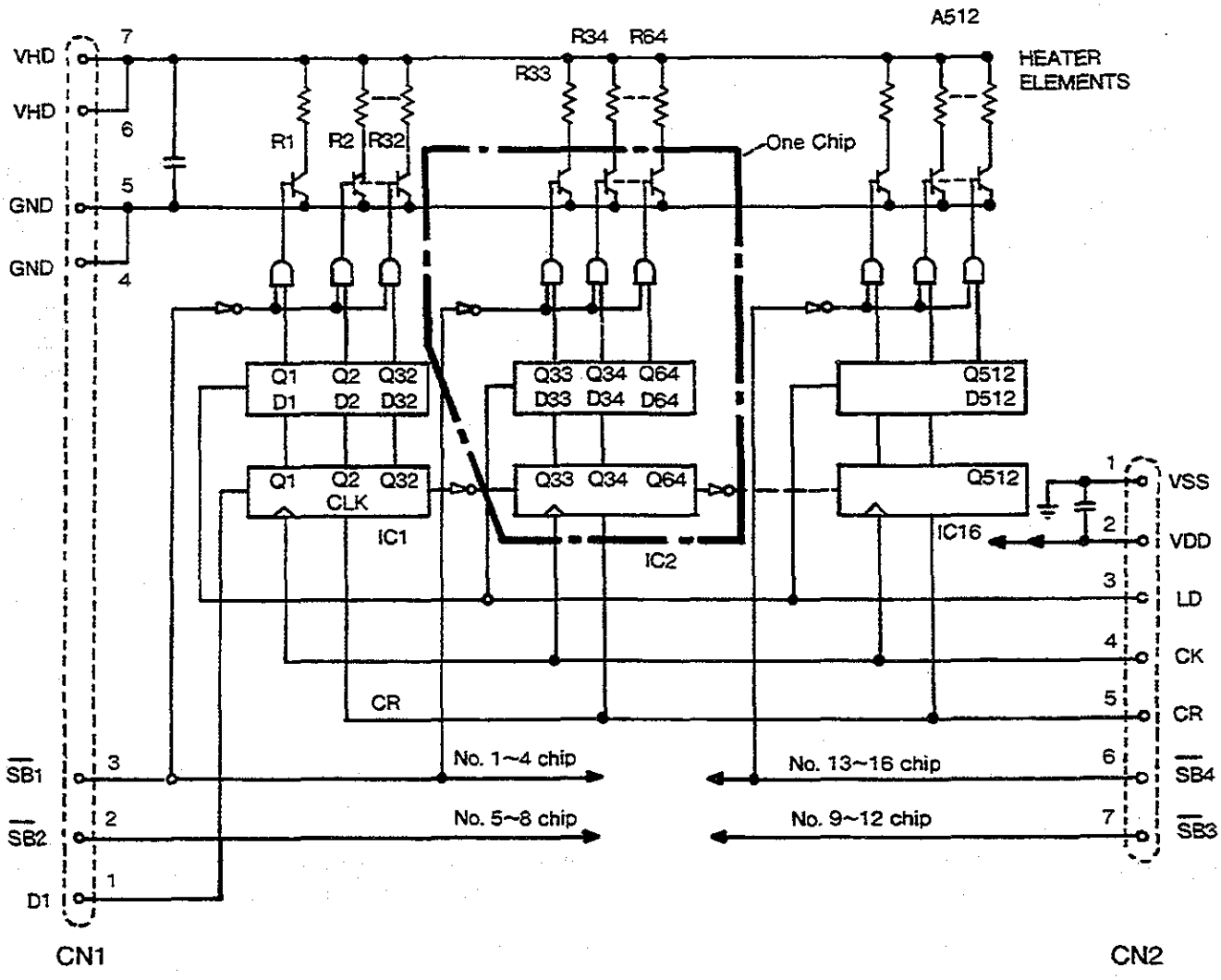
Recorder software accepts FHR and UA data from the supervisor CPU and computes the vertical coordinates along the slice where the dots for each channel are to be outputted. The corresponding printhead element is fired each time the motor steps.

Alphanumerics Mode

The recorder CPU accepts inputs from either the supervisor CPU or the Keypad or Keyboard in the form of message pointers and any associated data. The CPU then builds the message character string (along with a string for any data) and stores it in a memory buffer in preparation for printing. The CPU then uses a look-up table to determine which dots to fire to form the characters which make up the strings.

Test Mode

When the recorder test is initiated, the vertical lines are printed by stopping the motor and printing all 512 dots in 8 blocks of 64. (This lessens the drain on the power supply since firing all 512 dots at once could result in a maximum current of approximately 20 A.)



PRINTHEAD SCHEMATIC
FIGURE 4-1

PRINTING SEQUENCE

Timing is handled by interrupt-driven routines (RST 7.5) and hardware. The interrupt is driven by the PIA TIMER OUT port which is initialized in the continuous square-wave mode as a divide-by-8 counter clocked by TIMER IN. Therefore, TIMER OUT is a square wave with a period of 890 µs (1/(9 kHz/8)). The sequence for printing a dot slice is as follows:

1. 64 8-bit words representing dot-slice data are stored in a temporary buffer.
2. The stepping motor advances the paper.
3. The dot data is shifted into the printhead shift registers serially and the temporary buffer is cleared.
4. The strobe lines are driven low for 5 7.5-interrupt periods which enables the dot gates thus firing the printhead elements.
5. The next slice is loaded in the temporary buffer and held until the stepper-motor flag is set again.

Print-Sequence Hardware

The recorder software routine that outputs an 8-bit dot word to the printhead performs an I/O write to hex address E0 and loads the byte into parallel-in/serial-out shift register, U3. This initiates the following hardware operations:

1. The decoded address line (U13, pin 7) which loads in the byte also loads the preset values into the counter (U9 and U10).
2. This enables the counter (which is clocked by the 6-MHz system clock) by driving U15 (pin 6) high.
3. The counter (U9 and U10) then clocks in the dot data from U3 into the printhead shift registers.
4. When the 8 bits are shifted, the counter stops when U15 (pin 6) goes low.

The foregoing sequence is summarized in the timing diagram shown in FIGURE 4-2. Note that when U15 disables the counter, Q2 of U9 (Dot Clock) is high. This is because the printhead shift register accepts a bit on the falling edge of its clock.

On the next byte load, when D7 appears at pin 9 of U3, the H→L transition clocks it in. When the clock goes high, D6 is shifted out to the printhead and clocked in on the next H→L transition.

The A/D process is for one word of a slice and must be repeated 64 times until all the slice dot-data is written into the printhead. When this occurs, the CPU transfers the 512 bits to the element latches with two I/O writes to U2 which drive pin 15 low and then high.

Stepper-Motor Hardware/Software

The stepper-motor is timed by an interrupt-driven (RST 7.5) routine which sets a flag when a preset software counter decrements to 0; the preset value being determined by the chart speed in use. Approximate stepping times are given in TABLE 4-8.

CHART SPEED	STEPPING TIME
1 cm/min	133 ms
3 cm/min	44 ms
25 cm/min Paper Advance	5 ms

STEPPING TIMES
TABLE 4-8

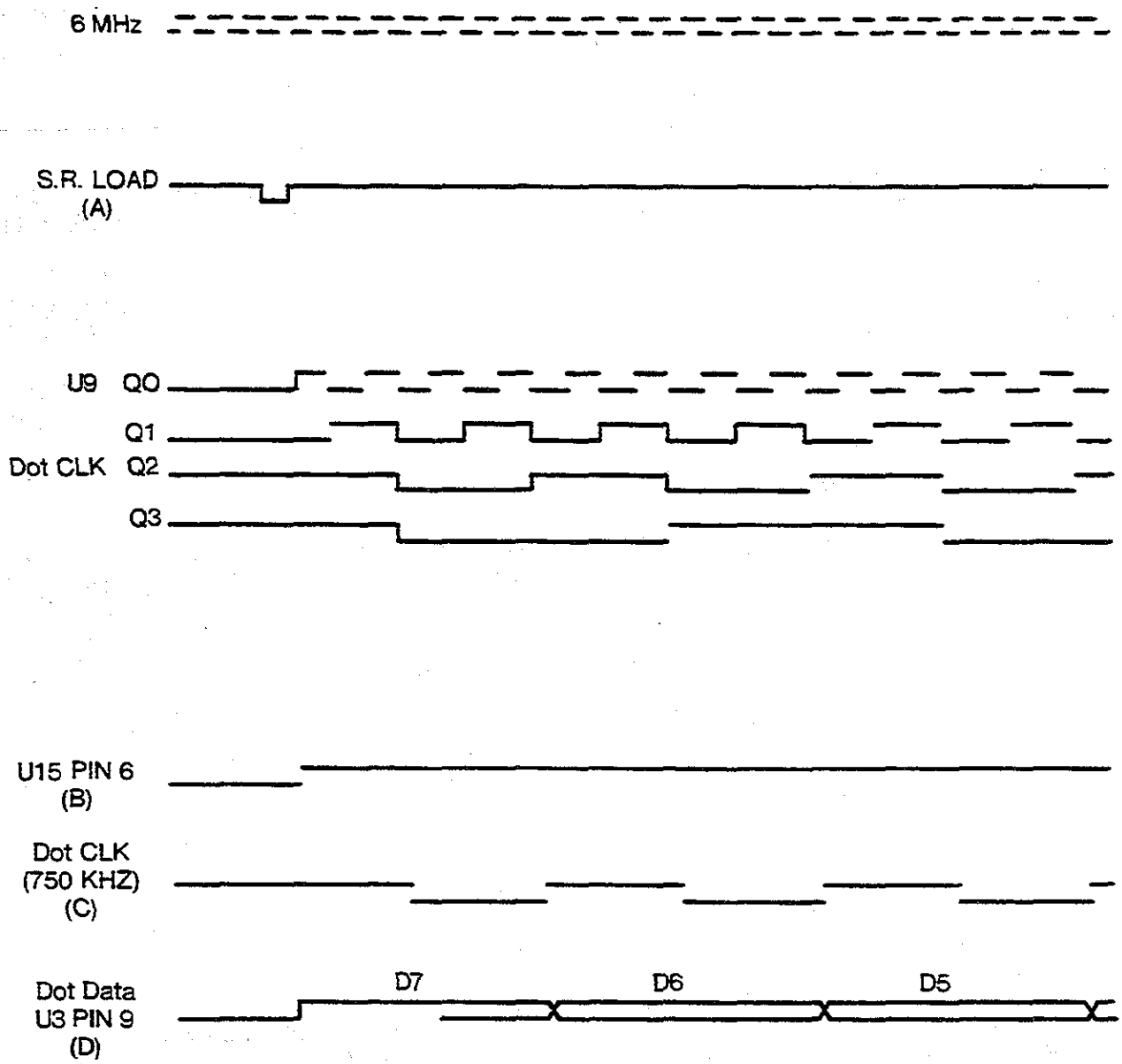
When the flag is set, another routine resets and initiates the following operations and routines:

1. The CPU performs two I/O writes to U20 (decoded 20 hexadecimal; U13, pin 14) which set and reset pin 7 (TP2) of U20 via the data writes (D bus). This steps the motor via comparator U18 and driver U19.
2. The CPU proceeds to the printing routine.

Printhead Firing

Once the motor has stepped, the CPU initiates the following routines:

1. The CPU loads in the dot-data slice.
2. The CPU determines if it can print (paper not being advanced) and if so, it enables a strobe flag and presets a software counter. On the next 7.5 interrupt, a routine causes the CPU to perform an I/O write to U2 (decoded 00 hexadecimal; U13, pin 15).
3. During power-up, U1 (pin 3) was cleared. When the CPU writes to U2 for the first time, it also sets U1 (pin 3) which drives U1 (pin 9) high. If U1 (pin 8) is also high (no head shutdown), U12 (pin 13) goes high, allowing strobe pulses through from U2 (pin 2).
4. During a write to U2, the CPU also sets U2 (pin 2). This drives U12 (pin 11) low, if enabled, which fires the printhead thermal elements via STB1-STB4. The strobe lines are held low until the software counter decrements to 0 (5, 7.5-interrupts or approximately 7 ms).



PRINT-SEQUENCE TIMING DIAGRAM
FIGURE 4-2

SUPERVISOR-TO-RECORDER CPU MESSAGES

Messages sent to the recorder CPU from the supervisor CPU are strings consisting of 8-bit words with a string length from 1 to 8 words. The messages fall into the following categories:

Alphanumerics

Alphanumerics refers to the messages and any associated data printed on the strip chart. (Message data currently limited to time/date information.)

HR and UA Values

These values are the heart rate and uterine activity data to be plotted on the strip chart.

Recorder Control Words

These represent the recorder commands from the front panel or supervisor sent via the REC b bus. These commands and their formats are shown in TABLE 4-9.

RECORDER COMMAND	HEXADECIMAL FORMAT
Recorder OFF	00
Recorder ON	FF
Recorder Speed Override	7F

RECORDER CONTROL WORDS
TABLE 4-9

Of particular importance in troubleshooting is to realize that Recorder ON/OFF and other functions are initiated in the supervisor software. Consequently, a recorder malfunction isn't necessarily limited to the recorder and Recorder Board. Failure to transmit the correct control words by the supervisor CPU will also result in malfunctions even though the recorder is functioning properly.

MESSAGE FORMAT

The supervisor CPU sends messages to the recorder in the format outlined in TABLE 4-10 A. Bytes 0-7 are summarized as follows:

Byte 0

This byte is used as a control word to identify the message being sent through the hexadecimal codes 01-0C.

Byte 1

This byte is related to the message identified by Byte 0 and will represent recorder control, mode-change ID, pressure data, or heart rate data.

Byte 2

This is the mode-change message byte for messages 1, 4, or 8.

Bytes 3, 4, 5, 6, and 7

These bytes indicate minutes, hours, day, month, and year, respectively for messages 1, 4, and 8.

MESSAGE #	BYTE # — FORMAT	USE
01 04 08	0 — Control Word (01, 04, 08) 1 — Recorder Control: 00H = Recorder OFF FFH = Recorder ON 7FH = Speed Override 2 — Display Mode 2* 3 — Minutes (0 – 59) 4 — Hours (0 – 23) 5 — Days (0 – 31) 6 — Months (0 – 12) 7 — Years (0, 83 – 99)	Recorder ON/OFF Print initial mode, time/date Print 10-minute updates Note: A zero (0) will be sent for day, month, or year if the user sets incorrect time.
02	0 — Control Word (02)	Start self-test
03	Not Used	
05	0 — Control Word (05) 1 — Recorder Control: 00H = Recorder OFF FFH = Recorder ON 7FH = Speed Override	Recorder ON/OFF Speed Override
06	0 — Control Word (06)	UA Reference auto-zero
07	0 — Control Word (07) 1 — Display Mode*	Print mode change
09	0 — Control Word (09) 1 — Pressure Data (0 – 100, 128)	Print Pressure Graphics Note: 128 is the value for pressure penlift.
0A	0 — Control Word (0A) 1 — Heartrate Data (0, 30 – 240)	Print Heartrate Data graphics Note: Zero (0) is the value for heartrate penlift.
0B	0 — Control Word (0B)	Battery Failure Print SET TIME/DATE
0C	0 — Control Word (0C)	Print BASELINE PRESSURE OFF-SCALE

*The display mode format is shown in TABLE 4-10 B.

SUPERVISOR-TO-RECORDER MESSAGES
TABLE 4-10 A

HR MODE**	MESSAGE PRINTED
x0H	CARDIO INOP
x1H	FECG
x4H, x3H	US
x4H – xFH	PNONO
UA MODE**	
0xH	UA INOP
2xH	IUP
1xH, 3xH	TOCO
4xH – FxH	TELEMETRY

**x = don't care

DISPLAY MODE FORMAT
TABLE 4-10 B

4.4 DUAL-CARDIOTACH BOARDS — THEORY OF OPERATION

4.4.1 CORRELATOR BOARD (7180)

The Correlator PCB Board (7180) uses a 6-MHz Z-80 processor. The analog and digital sections of the 7180 Board and their respective functions are discussed below:

ANALOG SECTION

The ultrasound audio signal (15 V p-p) is input to the 7180 Board at card Edge Pin Ⓨ. From this point, the signal is attenuated 40 dB by resistors R31 and R32. This signal is then fed through the filter chain created by U33 (pins 1-3, 5-7, 8-10). These amplifiers form a bandpass filter from 200 — 400 Hz with a gain of 30 dB. The filter uses 4 poles at 200 Hz and 2 poles at 400 Hz. This modified US audio signal is the feed into pin 15 of analog switch U11.

The phono signal from the 5800 Multifunction Board enters on Pin Ⓩ of the edge connector and is amplified by 20 dB before being fed into U11 (pin 2).

Using a signal from latch U5 (see below) either the US or PHONO signal is selected by U11 and fed into AGC amplifier U7 after first being attenuated by 15 dB by R14 and R15. The AGC amp will attempt to maintain an output voltage of 250 mV p-p over the input range of 75 mV p-p to 15 V p-p. The attack time-constant is set by C17 and C18. The decay time is set by R16.

The output of the AGC is half-wave rectified by U12 (pins 12, 13, 14). This rectifier has a gain of 23.5 dB. After rectification, the signal is fed to U12 (pins 8, 9, 10) which serves as the envelope filter. This is a 2-pole Bessel low-pass filter with a 20 dB gain and a cutoff frequency of 20 Hz. The envelope signal is then fed to pin 7 of analog switch U11. The output of the AGC is also fed into U12 (pins 1, 2, 3) to provide an ACG phono signal for use by the audio on the Multifunction Board. The ACG signal is amplified by 15 dB.

DIGITAL SECTION

The digital section of the 7180 Board consists of a Z-80 CPU (U1), 8K of ROM (U2), 2K of RAM (U3), timer chip (U4), latch (U5), decoder (U8) and A/D converter (U6). Additional logic is provided by a D flip-flop (U9) and a quad NAND gate (U10).

Timer chip U4 is used by the microprocessor to provide a 5-ms timing interrupt used to sample the input analog signal used for correlation. And secondly, it is used to determine if either TP1 or TP2 has been grounded. These two test points indicate to the processor that the user wishes to execute one of the internal self-tests contained within the PROM.

Consult the self-test section of this manual (Section 6) for a detailed description of these tests.

Decoder U8 is used to provide the chip selects needed by the other components in the system. It uses address lines A15 and A14 to provide 16K select lines whenever memory is addressed. In addition, the block of addresses from C000H to FFFFH are further decoded using address lines A0 and A1. The use of these chip selects is given in TABLE 4-11.

ADDRESS RANGE	USE
0000 – 3FFFH	ROM (U2)
4000H – 7FFFH	RAM (U3)
8000H – BFFFH	Latch (U5)
C000H – FFFFH	A/D Converter (U6), {if A0 = 1} DAC Test Board, {if A0 = 0}

CORRELATOR BOARD ADDRESS TABLE
TABLE 4-11

Whenever address range C000H to FFFFH is addressed, D flip/flop U9 generates 1 processor wait state. Latch U5 is used by the processor to provide a number of control signals for the system. Use of the latch bits are depicted in TABLE 4-12.

BIT NUMBER	USE
Q1	unused
Q2	unused
Q3	LED (DS1)
Q4	EVENT OUT (to 6802)
Q5	US/PHONO select to A/D
Q6	US/PHONO signal to A/D
Q7	PHONO signal to AGC
Q8	US signal to AGC

LATCH/BIT ASSIGNMENT
TABLE 4-12

As discussed above, quad analog switch (U11) is used to control which signal is presented to AGC amp (U7) and whether the input to the A/D converter is the US signal or the PHONO signal.

4.4.2 CPU BOARD (6802)

The CPU Board is the supervisor of the Model 115 Fetal Monitor, providing the unit with dual-cardiotach capabilities. It accepts heartbeat event pulses, mode inputs, inputs from switches, and a frequency input from the pressure channel. It calculates heart rate and uterine pressure. It sends heart rate and uterine activity data to the Display and Recorder Boards. In addition, it sends time/date and message codes to the Recorder.

The processor is an 8085 running at 6.144 MHz. A 27128, 128-K PROM holds the program. 256 bytes of static RAM reside in an 8155 and 50 bytes of battery-backed RAM reside in U27. Device select pulses are generated by a pair of 74F138 3-to-8 decoders (U8 and U9).

The I/O ports on two 8255s and one 8155 provide most of the I/O to/from the edge fingers. A MDAC (U14) and an OP-AMP (U13) control the audio volume. The battery-backed real-time clock chip (U27) provides time and date data to the processor.

TIME BASES

U10 sends the 6.144 MHz clock to the 8085 and to the Recorder Board via 18. U1-U3 supply time bases to the ECG Board and the Recorder Board, as well as drive the 8085 RST 7.5 pin at 1.123 kHz. The 8085 uses this signal as a time base for processing. Y2 and U26 oscillate at 32.768 kHz to provide a time base to the real-time clock (U27).

Device Select Logic

The device select pulses are generated by a pair of 3-to-8 decoders (U8 and U9). U8 selects I/O devices and U9 selects memory devices. The conditions required for selection of each device are shown in TABLE 4-13.

IO/M	A15	A14	A13	A12	DEVICE SELECT NAME	DEVICE SELECT LOGIC
0	0	0	0	X	YOM	U12 (PROM)
0	0	0	1	X		*
0	0	1	0	0	MP1	U22 (RAM)
0	1	0	0	0		U27 (CLOCK CHIP)
1	0	0	0	0	MP1	U22 (I/O or TIMER)
1	0	0	0	1	Y1P	U7 (I/0)
1	0	0	1	0	Y2P	U23 (I/O)
1	0	0	1	1	Y3P	U14 (AUDIO DAC)
0	1	1	0	0		RTC

CPU DEVICE SELECTION
TABLE 4-13

*This combination of address lines will occur only in the event of a bus error. If the combination does occur (i.e. due to static discharge), U15 (pin 35, ready) will go low, freezing the 8085 and preventing it from overwriting time/date information in the Real-Time Clock (U27). In approximately .5 seconds the Watchdog Timer will time out and restart the processor.

ADDRESS LATCH AND PROM

Unlike all other bus-connected devices on the 6802 Board, the PROM (U12) does not contain address latches to demultiplex the address/data lines, AD0-AD7. U11 latches A0-A7 from AD0-AD7 lines at the falling edge of ALE. A0-A7 and A8-A13 address any of the 16K bytes in the PROM.

CLOCK CALENDAR

The battery-backed clock/calendar chip (U27) also contains 50 bytes of battery-backed RAM. The 4-volt battery is located in the chassis, not on the board. The 32.768 kHz time base for the clock is generated by U26, Y2, and associated components.

When the monitor is turned off, U26 and U27 are powered by the battery through Q2. Q2, Q7, D1, and associated components disconnect U26 and U27 from the battery if the battery voltage drops below 3.85 V. Low battery voltage can occur if the monitor is placed in storage for several weeks.

This circuit keeps the battery from being severely discharged which would impair its ability to hold a charge.

R39 is set so the right side of the differential pair (Q7) will draw current through the Q2 base whenever the battery voltage is 3.85 V or greater. Thus, Q2 is kept on and battery power is provided to U26 and U27. If the battery voltage drops below 3.85 V, the voltage at Q7 (pin 5) will be below the 2.5 V at Q7 (pin 2), provided by reference diode D1. The right side of Q7 will then stop conducting and Q2 will turn off. The remaining load from the battery is thereby removed.

When power is applied to the monitor, D2 provides power to U26 and U27. The battery is charged through D3 and R66.

U27 (pin 22) detects losses of battery power. If battery power has been lost, U27 (pin 22) will be held low by C50 at the instant of power-up. This low state will clear a flag in U27. Shortly after power-up, the 8085 will interrogate this flag. If it has been cleared, the 6802 Board sends a code to the Recorder Board to print the message "SET TIME/DATE" on the chart paper. This message is repeated until a valid time and date are set according to the procedure described in Section 3.3.

U5 is required for reliable operation of U27. U5 is a transparent latch which conditions the chip enable for U27 by blocking it until the occurrence of a rising edge at ALE. Q3 ensures that battery current is not drained by the chip enable circuitry when the monitor is off. TABLE 4-14 shows which signals are applied to the 6802 Board in respect to the Time/Date setting switches.

CPU EDGE FINGER	NAME	PORT
Ⓑ	TD ENABLE	U23, PA7
R	TD SEL	U23, PC7
13	TD ↓	U23, PC6
P	TD ↑	U23, PC5

TIME/DATE SETTING SWITCH SIGNALS
TABLE 4-14

INITIALIZATION AND POWER-ON RESET

A shunt regulator (D4) along with Q4, and associated resistors form part of a reset circuit. When the 5-V supply line is less than approximately 4.7 V, D4 does not conduct and Q4 is off. U27 is held reset by R68 and R69, U27-chip-enable is inhibited since Q5 is off, and the 8085 is held reset because there is no voltage on C58. The 8085, in turn, keeps other devices reset via its reset output (U15, pin 3). When the 5-V supply line exceeds 4.7 V, D4 conducts which takes U27 out of reset and allows C58 to begin charging through D5 and R83. When C58 charges to logic 1 (approximately 30 ms), the 8085 is no longer held reset and its reset output goes low. Approximately 5 µs later, Q6 turns off, turning on Q5 thereby stopping the inhibit on U27-chip-enable. R89 provides hysteresis in the power-up circuit. During power-down, when Q4 shuts off, A9 turns on which rapidly discharges C58.

Q6 is required since the state of U5 is indeterminate between the time power is applied to the board and U5 receives the first ALE pulse. When the 8085 comes out of reset, it addresses the PROM at address 00. The ALE pulse produced will initialize U5 (pin 2) to logic 0. A few microseconds later, Q6 shuts off, enabling the chip-enable circuitry for U27.

HEART RATE RELATED SIGNALS

The transducer assemblies, the leg-plate assembly, and the maternal ECG cable assembly, contain jumpers which pull the mode select lines down to 0 V when the transducers are connected. Thus, when the ultrasound (US) transducer is used, the 6802 Edge Finger Y is low. Similarly, when the phono transducer is used Z is low. If the ECG leg plate is connected, 21 is low, and 7 is pulled low by the maternal ECG cable. The 8085 polls U20 (a hex 3-state bus driver) to determine the mode(s) selected.

Heartbeat event pulses, from the 5807 ECG Board, drive RST 5.5 on the 8085 via Edge Finger E. Phono and ultrasound heartbeat event pulses from the 7180 Board drive RST 6.5 on the 8085 via Edge Fingers Ⓘ and 6.

DS3 and DS2 flash for ultrasound/phono or ECG events respectively, providing an aid for troubleshooting. For every "valid" heartbeat of the displayed heart rate (see TABLE 4-15), Edge Finger 19 goes low for approximately 100 ms thereby flashing the heartbeat indicator on the Display Board.

The 8085 calculates the instantaneous heart rates from the interval between heartbeat event pulses. Heart rate is sent to the Recorder Board via U7 (Port A), to the Display Board (4-beat average) via U7 (Port B), and to the central station connector via U22 (Port A), U25 and U28 for heart rate 1, and via U14 and U30 for heart rate 2.

U25 is an 8-bit digital-to-analog converter whose output is offset and scaled by U28 and associated components to produce an analog output at V for heart rate 1. U14 is a dual digital-to-analog converter whose output is offset and scaled by U30 and associated components to produce an analog output at 15 for heart rate 2. These analog outputs are offset and scaled as shown below:

$$\text{Analog heart rate voltage} = (\text{heart rate}/100) - 1.2\ \text{V}$$

A strobe is provided for each heart rate channel to allow the analog heart rates to be digitized by an external data acquisition system. (See TABLE 4-15, to distinguish between heart rates 1 and 2.) Pin 13 and pin 23 on J102 (central station connector) provide signals HR1 XFER and HR2 XFER which originate at Edge Fingers Ⓟ and T, respectively, on the 6802 Board. When data from a new heart rate interval is available at one of the DACS, the respective HR XFER signal goes low while the analog output stabilizes. Approximately 100 ms later, the HR XFER signal rises. This rising edge may be used to strobe the data.

MODE	NAME	HR1 MODE VOLTAGE	HR2 MODE VOLTAGE
A	HR INOP	9.80 V to 10.20 V	0 ± 15 mV
B	US	5.037 V to 5.192 V	0 ± 15 mV
C	PHONO	5.037 V to 5.192 V	0 ± 15 mV
D	FECG	−4.31 V to −5.66 V	0 ± 15 mV
E	MECG	9.80 V to 10.20 V	9.690 V to 10.190 V
F	MECG & US	5.037 V to 5.192 V	9.690 V to 10.190 V
G	MECG & PHONO	5.037 V to 5.192 V	9.690 V to 10.190 V
H	FECG & US	4.88 V to 5.163 V	−4.650 V to −5.330 V
I	FECG & PHONO	4.88 V to 5.163 V	−4.650 V to −5.330 V

HEART RATE/MODE OUTPUT VOLTAGES
TABLE 4-15

In modes D and E of the Heart Rate Mode Voltages Table, Edge Finger [2] (U23, PB1) will pulse high for 100 ms for every ECG heartbeat event pulse.This causes the audio section of the Multifunction Board to produce a beep in the speaker. In modes F-I of the Heart Rate Mode Voltages Table, S1 controls whether or not ECG beeps will be superimposed on the ultrasound or phono audio. If the plunger on S1 is in the depressed position (on), ECG beeps will be superimposed on the ultrasound or phono audio. These beeps will be softer than those produced in modes D and E (see MULTIFUNCTION BOARD — THEORY OF OPERATION). If it is desired to inhibit the ECG beeps in modes F-I, the plunger on S1 can be moved to the "out" position.

When two successive heart rates differ by more than 25 bpm, or artifact is detected for either heart rate, 1 or 2, the Recorder Board will be sent information to interrupt the respective trace. An ECG trace will not be interrupted if the ECG ARTIFACT ELIMINATION switch is OFF (CPU Finger Ⓨ high). Successive heart rates that differ by more than 25 bpm will cause Edge Fingers Ⓧ (J102, pin 15) or [17] (J102, pin 19) to go high for heart rate 1 or 2, respectively. These signals are called HR1 PENLIFT 2 and HR2 PENLIFT 2, respectively, and can be used by a remote alert system. An open collector version of HR1 PENLIFT 2 is available at Edge Finger ㉑ (J102 pin 8) to drive the pen solenoid on a remote recorder. Penlift signals will not be produced in ECG mode if the ECG ARTIFACT ELIMINATION switch is in the OFF position.

Heart rate mode information is available for an external system via J102. Heart rate 1 mode information is sent to J102, pin 17 via edge pin ⑱, and heart rate 2 mode information is sent to J102, pin 1 via edge pin Ⓐ. The Heart Rate Mode Voltages Table summarizes the levels at J102 for the various heart rate modes.

UTERINE ACTIVITY RELATED SIGNALS

The mode inputs, DIRECT UA at Finger [A] and TOCO at Finger [F] come from the Multifunction Board. (This section refers to TABLE 4-16).

UA MODE	UA MODE
UA INOP	−3.788 V to −6.578 V
TOCO	8.907 V to 10.56 V
DIRECT UA	3.996 V to 5.76 V

(UA MODE OUTPUT VOLTAGES)
TABLE 4-16

The multifunction pressure section feeds CPU Finger ⑧ with a frequency in the range of 0 − 16.32 kHz. A change in frequency of 6528 Hz represents a 100 mmHg change in uterine pressure (or a change of 100 on the 0 − 100 TOCO scale). The frequency is applied to U22 (pin 3) which clocks the timer in U22. By reading and reinitializing the time at approxi-

mately an 8-Hz sampling rate, the 8085 derives the pressure value. This derived pressure value is relative to the value that was present when the Pressure Zero (UA REF) button was last pressed (the front-panel Pressure Zero button brings CPU Finger [12] low when it is activated).

The incoming frequency range that can be "zeroed" by the UA REF button is from 0 to 9792 Hz. A typical frequency in "direct" mode at 0 pressure is 3264 Hz.

The ± 1.2-V pressure signal at Finger [W] is derived from Port B of U22, which feeds a DAC (U24). The output current from the DAC is changed into a voltage by one section of U28. This analog voltage is available at J102 pin 2 and is offset and scaled as shown below:

$$\text{Analog Pressure Voltage} = (\text{Pressure}/41.67) - 1.2\text{V}$$

NUMERIC DISPLAY INTERFACE

The 6-digit multiplexed numeric readout is driven by 8 signals from the CPU Board. Refresh rate is approximately 60 Hz. BCD encoded numeric data is transmitted on U7 (PB0 – PB3). The digit strobes (XFER1 – XFER3) are produced by U7 (PB5 – PB7) and buffered by U4. The display strobe signal at [20] is used to strobe uterine activity numeric data present on U7 (PB0 – PB3) into a latch on the Display Board during the blank pulse (U7, PB4). Heart rate numeric data is present on U7 (PB0 – PB3) the remainder of the time.

RECORDER RELATED

U7 is used to send message codes and trending data to the Recorder Board. The Recorder Board drives the millidot thermal printhead which plots trending curves and prints messages on the chart paper. REC b_0 – REC b_7 send data while REC OBF and SUP ACK provide handshaking signals.When the 6802 Board has a data word to send to the Recorder Board, 6802 Finger Ⓢ (REC OBF) goes low. When the Recorder Board has accepted the data, it brings 6802 Edge Finger ⑯ (SUP ACK) low. After the cycle is complete, 6802 Fingers Ⓢ and [16] are high.

If the Recorder Board does not respond to REC OBF with SUP ACK within a reasonable time, the 6802 Board assumes the Recorder Board has malfunctioned and traps it by bringing Finger Ⓤ (REC TRAP) high (U22, pin 39).

The message codes are provided in Section 4.4.3, RECORDER BOARD — THEORY OF OPERATION. A variety of recorder related signals are found in TABLE 4-17.

ELECTRONIC VOLUME CONTROL

The audio volume of the monitor is controlled by U14, an 8085 compatible MDAC with internal data latches. The 8085 sends a data word from 0 (volume off) to 255 (maximum volume, no attenuation) to the DAC in response to the front-panel volume control pushbuttons. Holding down the Volume Up pushbutton (Finger [14] low) decreases the attenuation from Finger ⑬ to ㉔, whereas, the Volume Down pushbutton (Finger Ⓢ low, when activated) increases the attenuation.

WATCHDOG TIMER

U31 is a counter which monitors operation of the microprocessor and restarts it in the event of a malfunction (ie., due to static discharge).

U31 is clocked by an 8-Hz square wave at pin 1. Normally, the processor will continuously send reset pulses (rep-rate > 2 Hz) to U31 (pin 2) via U7 (pin 22), C63 and R92.These pulses reset U31 before U31 (pin 9) has a chance to go high. Since U31 (pin 9) is normally low, Q8 is off and the Watchdog Timer circuit has no effect.

If the processor malfunctions, it will not be able to send reset pulses to U31. In 500 ms, U31 (pin 9) will go high, turning on Q8 which will turn off D4 and Q4 thereby allowing C58 to be discharged by Q9. U15 (pin 36, RESET IN) will then go low, resetting the processor (U15). When the processor is reset, U15 (pin 3) goes high, thereby resetting U31 via R91 and R92. U31 (pin 9) then goes low, allowing U15 to come out of reset and to begin program execution from the power-up condition.

CPU EDGE FINGER	NAME	DESCRIPTION
11	RECORD	Senses front-panel Record button activation. The Recorder Board is sent the ON or OFF message via U7 (Port A).
X	RECORD LED	Activates the front-panel record LED.
⑰	SUP PAPER LOW	From Recorder Board. Causes the record LED to flash (if the recorder is ON).
⑲	SUP PAPER OUT	From the Recorder Board. Causes the CPU Board to latch the recorder status to OFF.
Ⓣ	PAPER ADV	From the Display/SW Board. Causes recorder to advance paper at 25 cm/min. Twenty seconds after a low-to-high transition, the CPU sends the following information to the recorder via U7 (Port A): Mode Information Time and Date Chart Speed
Ⓕ	SUP READY TO REC	From the Recorder Board. It goes low during recorder self-test. A low-to-high transition signals the CPU Board that the recorder test is complete. The CPU Board will trap the Recorder Board via CPU Finger Ⓤ if for any reason Ⓕ stays low for an unreasonably long period of time.
9	SPEED OVERRIDE	From rear-panel connector J102. If this line is held low for at least 120 ms and then brought high, the CPU will send a mesage to the recorder Board (via U7, Port A) to run the recorder stepper-motor at its highest trending speed.

RECORDER RELATED SIGNALS
TABLE 4-17

TELEMETRY

If the **Model 320 Telemetry** unit is properly connected to the 115 Fetal Monitor and is powered, the CPU Board will send the code to the Recorder Board to print the word "TELEMETRY" on the chart paper. This code will be sent only if the following conditions are met:

1. Telemetry at CPU Finger ⑦ is low.
2. ECG at CPU Finger 21 is low.
3. TOCO at CPU Finger F is high.

4.4.3 RECORDER BOARD (6665)

NOTE: Refer to Section 10.1 for the RS-232C Serial Interface Guide for the 6666 Recorder Board. Refer to Sections 10.2 through 10.4 for the Theory of Operation, including RS-232C and COROLAN Interface Guides, for the 7383C and 7383D Recorder Boards.

The Recorder Board plugs into the card cage Motherboard. Three plugs on the board itself provide the following interfaces:

1. P17: This plug accepts the connector for the optional 2115 Keypad or 2116 Keyboard.
2. P18: This plug accepts the connector for the recorder stepper-motor.
3. P19: This plug accepts the connector for circuits performing the following six functions:
   - Thermal printhead element power (Vhd).
   - Printhead serial-in/parallel-out shift registers and controls (DOT CLK, DOT DATA, and LOAD).
   - Printhead enable strobes, (STB0-STB4).
   - Power for PAPER LOW and PAPER OUT optosensors (OPTO DRIVE A and OPTO DRIVE B).
   - Opto-sensor outputs for PAPER LOW and PAPER OUT.
   - Printhead electronics power (+5 V).

HARDWARE/SOFTWARE

Hardware and software on the Recorder Board perform the following functions:

1. Accept message pointers, HR data, and UA data from the Supervisor CPU Board for printing on the strip chart.
2. Accept message pointers and patient data entered from the optional 2115 Keypad or 2116 Keyboard.
3. The recorder processor builds the message string (and any data string) and determines the line where the string(s) will be printed. Also,the software computes the graphics dot positions from the HR and UA data.
4. Step the recorder chart-paper motor, load alphanumerics and graphics dot patterns into the printhead, and fire the dot elements in the printhead.

Microprocessor

The microprocessor (U5) is an 8085, timed by the 6-MHz clock on the main CPU Board. The LSB's of the address bus (A0-A7) are strobed and latched into U7.

Combined with A8-A12, these lines form the 13-bit address bus permitting access to blocks of memory with a maximum of 8K storage.

The three high-order bits (A13-A15) select the memory or I/O peripheral to be accessed (partial decoding) via U13 and U14. Memory consists of 2 K of RAM (U8) and two 64-K ROMs (U9-U10). I/O peripheral devices include the 8155 RAM I/O timer (U6) used as an I/O port and 7.5 RST interrupt timer. U29 is an 8-bit input port which accepts message pointers and data relating to message, HR, and UA sent from the Supervisor CPU. U6 and U28 are used to manage handshaking with the CPUs of the Supervisor and optional Keypad or Keyboard.

STEPPER-MOTOR/PRINTHEAD INTERFACING

The following subsections address the 6665 Board circuitry that is associated with control of the stepper-motor and printhead.

Printhead Protection Circuits

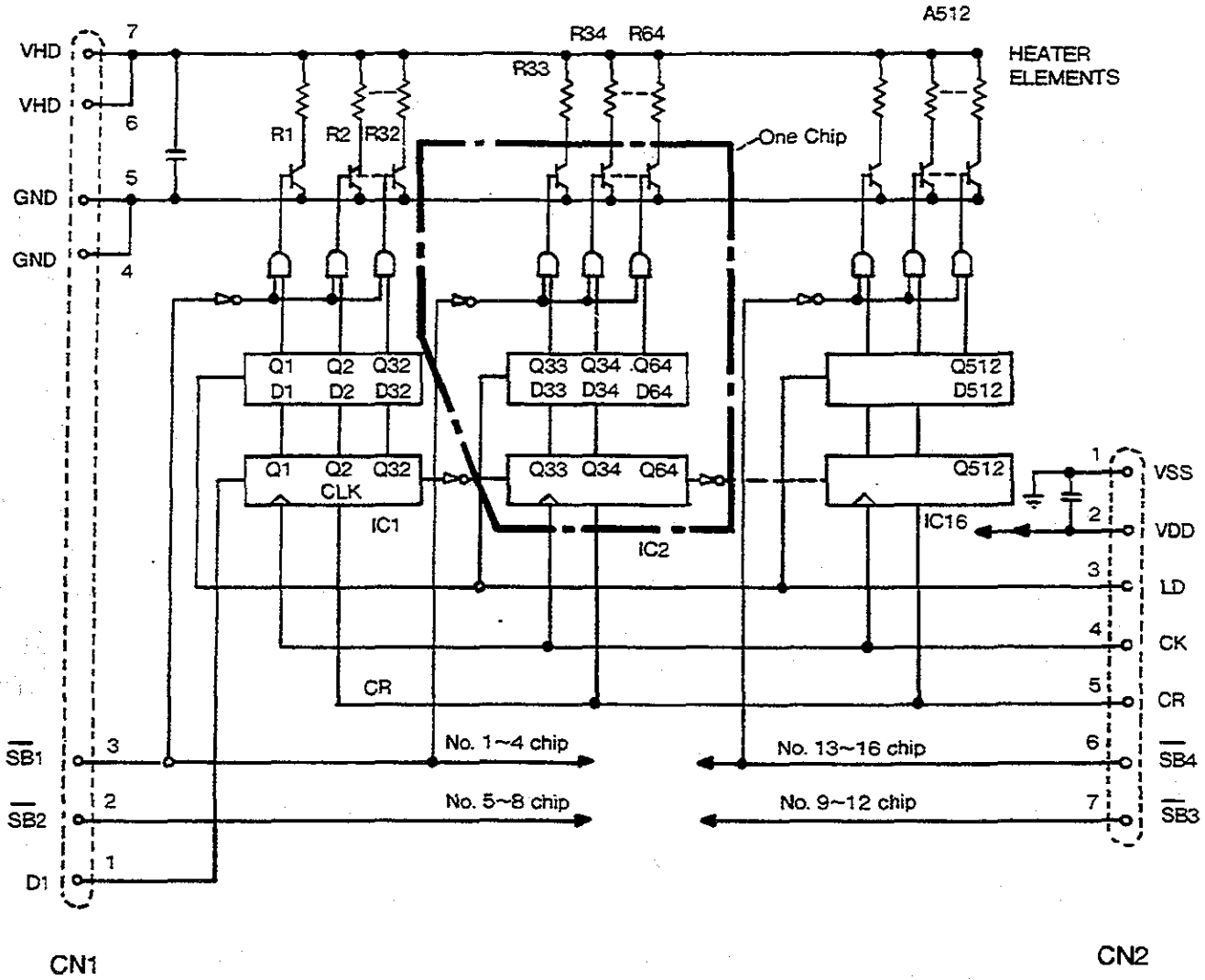
A thermal process is used to generate the dot pattern which makes up the graphics and alphanumerics on the strip-chart paper. Each dot is formed by one thin-film resistor element in a linear array of 512 elements across the printhead face. Because of the array density and the power required for each element, the maximum time an element can be energized is approximately 7 ms. To insure this time is not exceeded, both hardware and software measures are employed. The schematic diagram of the printhead is shown in FIGURE 4-3. The elements are represented by the line of resistors, R1-R512. Note that the supply bus (Vhd) to each element is switched by a series transistor controlled by an AND gate. The gate can only be enabled by one of the four strobe lines, STB0-STB4. In turn, strobe lines are enabled or locked-up high by hardware on the 6665 Board.

Power-Up Sequence

When monitor power is first turned on, R1 and C1 hold pin 6 of U21 (6665 Board) low for approximately 100 ms. At power-up, the supervisor processor (6802 Board) produces a "Reset Out" signal to the recorder CPU (U5, 6665 Board) which tri-states its address bus. Pull-up resistors RN5 pull the bus high which insures a high at U14 (pin 15) regardless of the states of its enable lines during at least part of the 100 ms period when pin 6 of U21 is held low. This sets the U21 flip-flop pin 3 low, which disables the strobe lines until the first I/O write to address OxH or 1xH (x = don't care, H = hexadecimal).

Once the recorder CPU has been reset, it can clear the printhead shift registers and the printhead gate-enable latches with an LD pulse. (This action prevents the writing of a random string of dots on the strip chart when the recorder is activated.)

When the recorder CPU is not printing data on the strip chart, pin 2 of U27 is low which holds counter U11 reset. When the CPU fires the printhead elements, and the strobe lines go low, U11 begins counting. If the strobe lines remain low in excess of 7 milliseconds, Q6 of U11 goes high which also disables the counter clock and drives the head shut line high. This action shuts down the printhead power supply which prevents any possible damage to the thermal elements.



PRINTHEAD SCHEMATIC
FIGURE 4-3

In a properly operating system, a head shutdown occurs if any of the strobe lines (TP5) are grounded for more than 7 ms. However, note the following precaution.

CAUTION: **Avoid grounding the strobe lines (TP5)** in the event of a **recorder malfunction** since U11 will not trigger a head shutdown if the IC is defective, or if it is not receiving a 9-kHz clock pulse.

Paper-Out/Paper-Low Alerts

A paper-out condition will also initiate a head shutdown and it will alert the recorder CPU via I/O port-PB7 (pin 34, U6). The recorder CPU will shut off the stepper-motor and signal the supervisor CPU via SUP PAPER OUT (U6, PC3 pin 1) of the condition. The supervisor CPU will shut off the front-panel "Record" LED and will not respond if an attempt is made to activate the recorder by depressing the Record pushbutton. Once the PAPER LOW optosensor encounters the black squares on the strip chart, it cuts off and pin IO of U4 goes high. This drives the output of the comparator (pin 13) low, which controls I/O port-PB6 (U6, pin 35).

This allows a software counter to increment by 3 for each time the stepper-motor routine runs. If "white" is detected, the counter is decremented by 1. This suppresses a false PAPER LOW alert (sometimes caused by a small imperfection within the paper itself) while initiating a PAPER LOW alert when the paper advances approximately halfway through the first black square.

PRINTHEAD MODES

Dot data must be presented to the thermal-element gates for each slice of chart paper; a slice being one step of the recorder chart-drive motor. Data is printed via the slices in one of three modes:

Graphics Mode

Recorder software accepts FHR and UA data from the supervisor CPU and computes the vertical coordinates along the slice where the dots for each channel are to be outputted. The corresponding printhead element is fired each time the motor steps.

Alphanumerics Mode

The recorder CPU accepts inputs from either the supervisor CPU or the Keypad or Keyboard in the form of message pointers and any associated data. The CPU then builds the message character string (along with a string for any data) and stores it in a memory buffer in preparation for printing. The CPU then uses a look-up table to determine which dots to fire to form the characters which make up the strings.

Test Mode

When the recorder test is initiated, the vertical lines are printed by stopping the motor and printing all 512 dots in 8 blocks of 64. (This lessens the drain on the power supply since firing all 512 dots at once could result in a maximum current of approximately 20 A.)

PRINTING SEQUENCE

Timing is handled by interrupt-driven routines (RST 7.5) and hardware. The interrupt is driven by the PIA TIMER OUT port which is initialized in the continuous square-wave mode and as a divide-by-8 counter clocked by TIMER IN. Therefore, TIMER OUT is a square wave with a period of 890 µs [1/(9 kHz/8)].

The following represents the sequence for printing a dot slice:

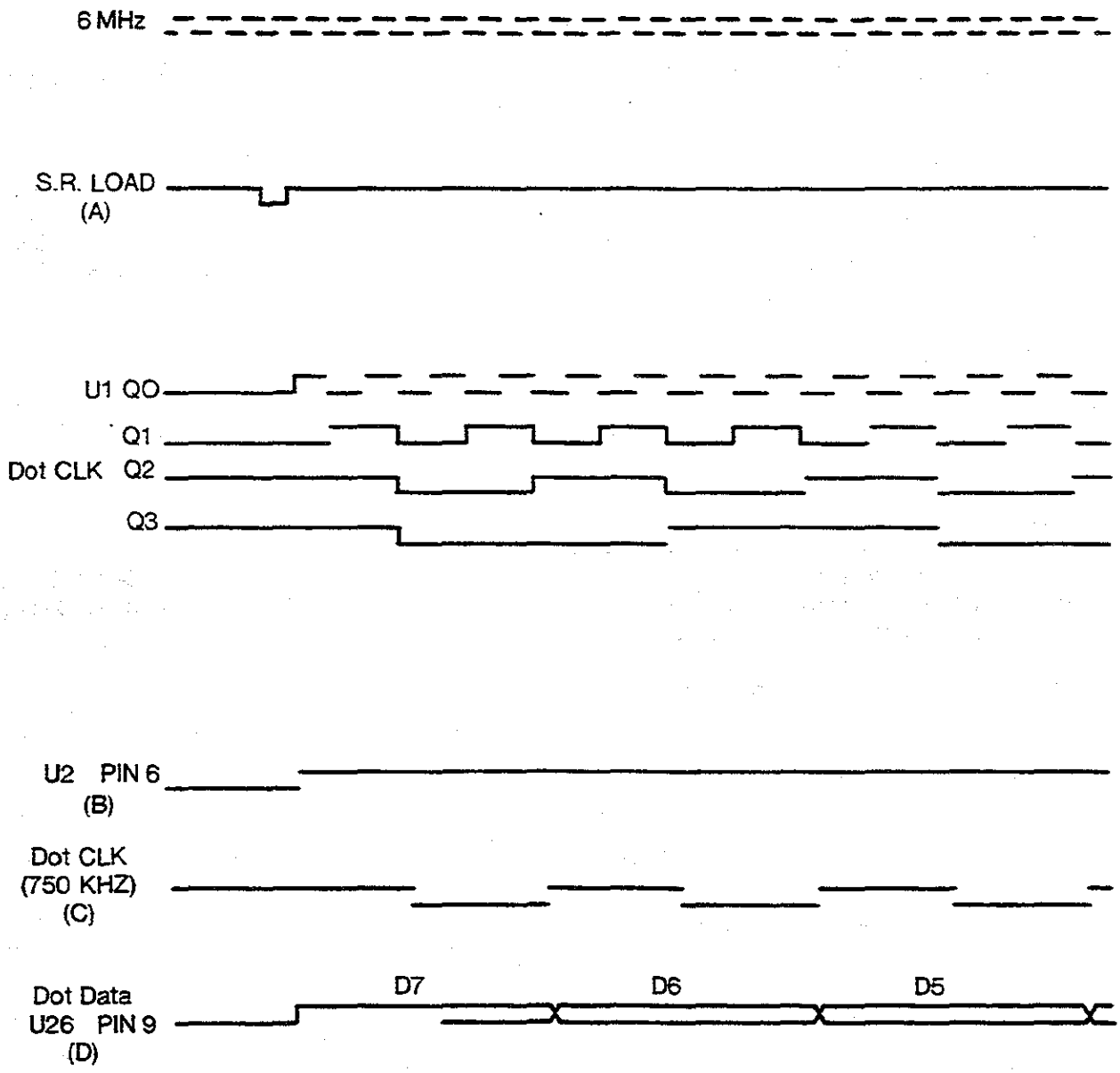
1. 64 8-bit words representing dot-slice data are stored in a temporary buffer.
2. The stepper-motor advances the paper.
3. The dot data is shifted into the printhead shift registers serially and the temporary buffer is cleared.
4. The strobe lines are driven low for five (5) 7.5-interrupt periods which enables the dot gates thus firing the printhead elements.
5. The next slice is loaded in the temporary buffer and held until the stepper-motor flag is set again.

Print-Sequence Hardware

The recorder software routine that outputs an 8-bit dot word to the printhead performs an I/O write to hex address E0 and loads the byte into parallel-in/serial-out shift register, U26. This initiates the following hardware operations:

1. The decoded address line (U14, pin 7) which loads in the byte also loads the preset values into the counter (U1, U3).
2. This enables the counter (which is clocked by the 6-MHz system clock) by driving U2 (pin 6) high.
3. The counter (U1, U3) then clocks in the dot data from U26 into the printhead shift registers.
4. When the 8 bits are shifted, the counter stops when pin 6 of U2 goes low.

The foregoing sequence is summarized in the timing diagram shown in FIGURE 4-4. Note that when U2 disables the counter, Q2 of U1(pin 12), DOT CLK is high. This occurs because the printhead shift register accepts a bit on the falling edge of its clock.



PRINT-SEQUENCE TIMING DIAGRAM
FIGURE 4-4

On the next byte load, when D7 appears at U26 (pin 9), the H→L transition clocks it in. When the clock goes high, D6 is shifted out to the printhead and clocked in on the next H→L transition.

The A/D process is for one word of a slice and must be repeated 64 times until all the slice dot-data is written into the printhead. When this occurs, the CPU transfers the 512 bits to the element latches with two I/O writes to U27 which drive pin 15 low then high.

Stepper-Motor Hardware/Software

The stepper-motor is timed by an interrupt-driven (RST 7.5) routine which sets a flag when a preset software counter decrements to 0; the preset value being determined by the chart speed in use. Approximate stepping times are listed in TABLE 4-18.

CHART SPEED	STEPPING ADVANCE
1 cm/min	133 ms
3 cm/min	44 ms
25 cm/min (Paper Advance)	5 ms

STEPPING TIMES
TABLE 4-18

When the flag is set, another routine resets and initiates the following operations and routines:

1. The CPU performs two I/O writes to U28 (decoded 20 hexidecimal) which set and reset pin 7 (TP2) of U28 via the data writes (D bus).
2. The above steps the motor via comparator U4 and driver U20.
3. The CPU then proceeds to the printing routine.

Printhead Firing

Once the motor has stepped, the CPU initiates the following routines:

1. The CPU loads the slice dot data.
2. The CPU then determines if it can print (paper not being advanced) and if so, it enables a strobe flag and presets a software counter. On the next 7.5 interrupt, a routine causes the CPU to perform an I/O write to U27 (decoded 00 hexadecimal; pin 15, U14).
3. During power-up, pin 3 of U21 was cleared. When the CPU writes to U27 for the first time, it also sets pin 3 of U21 which drives pin 9 of U21 high. If pin 8 of U21 is also high (no head shutdown), pin 13 of U12 goes high, allowing strobe pulses through from pin 2 of U27.
4. During a write to U27, the CPU also sets U27, pin 2. This drives pin 11 of U12 low (if enabled) which fires the printhead thermal elements via STB1-STB4. The strobe lines are held low until the software counter decrements to 0 (five 7.5 interrupts or approximately 7 ms).

SUPERVISOR/RECORDER CPU MESSAGES

Messages sent to the recorder CPU from the supervisor CPU are strings of length from 1 to 8 bytes. The messages fall into the following categories:

Alphanumerics

Alphanumerics refers to the messages and any associated data printed on the strip chart (message data currently limited to time/date information).

HR/UA Values

These values are the heart rate and uterine activity data to be plotted on the strip chart.

Recorder Control Words

These represent the recorder commands from the supervisor sent via the REC b bus. Of particular importance in troubleshooting is to realize that Recorder ON/OFF and other functions are initiated in the supervisor software. Consequently, a recorder malfunction isn't necessarily limited to the recorder and Recorder Board. Failure to transmit the correct control words by the supervisor CPU will also result in malfunctions even though the recorder is functioning properly.

MESSAGE #	BYTE # — FORMAT	USE
00	0 — Control Word (00) 1 — Display Mode 1* 2 — Display Mode 2*	Print RS-232C mode changes
01 04 08	0 — Control Word (01, 04, 08) 1 — Recorder Control: 00H = Recorder OFF FFH = Recorder ON 7FH = Recorder Speed Override 2 — Display Mode 1* 3 — Display Mode 2* 4 — Minutes (0 – 59) 5 — Hours (0 – 23) 6 — Days (0 – 31) 7 — Months (0 – 12) 8 — Years (0, 83 – 99)	Initialization Recorder ON/OFF Print initial mode, time/date Print 10-minute updates Note: A zero (0) will be sent for day, month, or year if the user sets incorrect time.
02	0 — Control Word (02)	Start self-test
03	Not Used	
05	0 — Control Word (05) 1 — Recorder Control: 00H = Recorder OFF FFH = Recorder ON 7FH = Recorder Speed Override	Recorder ON/OFF Speed Override
06	0 — Control Word (06)	UA Reference auto-zero
07	0 — Control Word (07) 1 — Display Mode 1*	Print 20-sec Mode 1 change
09	0 — Control Word (09) 1 — Pressure Data (0 – 100, 128)	Print Pressure Graphics Note: 128 is the value for pressure penlift.
0A	0 — Control Word (0A) 1 — Heartrate Data 1 (0, 30 – 240)	Print Heartrate Data 1 graphics Note: Zero (0) is the value for heartrate penlift.
0B	0 — Control Word (0B)	Battery Failure Print SET TIME/DATE
0C	1 — Control Word (0C)	Pressure off-scale
0D	0 — Control Word (0D) 1 — Heartrate Data 2 (0, 30 – 240)	Print Heartrate Data 2 graphics Note: Zero (0) is the value for heartrate penlift.
0E	0 — Control Word (0E) 1 — Display Mode 2*	Print 20-sec Mode 2 change

*The display mode format is found in TABLE 4-19 B.

SUPERVISOR-TO-RECORDER MESSAGES
TABLE 4-19 A

MESSAGE FORMAT

The supervisor-to-recorder CPU messages are outlined in TABLE 4-19 A. Bytes 0-8 are summarized as follows:

Byte 0

This byte is used as a control word to identify the message being sent through the hexadecimal codes 00-0E.

Bytes 1 and 2

These bytes are related to the message identified by Byte 0 and may represent recorder control, mode-change ID (display mode 1 or 2), pressure data, or heart rate data (HR 1 or HR 2).

Byte 3

This is the mode-change ID message byte (display mode 2) for messages 1, 4, or 8.

Bytes 4, 5, 6, 7, or 8

These bytes indicate minutes, hours, day, month, and year respectively, for messages 1, 4, or 8.

4.5 ANALOG/DIGITAL SIGNALS SUMMARY

This section contains a comprehensive listing (TABLE 4-22) of all signals (analog and digital) referred to throughout the manual's text, block diagrams, and schematics. Legend definitions for signal type and digital format are given in TABLES 4-20 and 4-21, respectively. The principal data and control signals are illustrated in the signal flow graph, FIGURE 4-5.

HR 1 MODE**	HR 2 MODE**	MESSAGE PRINTED
x3H	xCH	CARDIO INOP
x1H	xCH	US ∿∿
x2H	xCH	PHONO ∿∿
x8H	xCH	FECG ∿∿
x3H	x4H	MECG ∿∿
x1H	x4H	MECG ∿∿ US ∿∿
x2H	x4H	MECG ∿∿ PHONO ∿∿
x1H	x8H	FECG ∿∿ US ∿∿
x2H	x8H	FECG ∿∿ PHONO ∿∿
UA MODE**		
0x		UA INOP
2xH		TOCO
1xH, 3xH		IUP
4xH – FxH		TELEMETRY

** x = don't care

DISPLAY MODE FORMAT
TABLE 4-19B

Signal Type	ID
A	Analog
D	Digital
PS	Special Power Supply
R	Reference Supply
SW	Switch

SIGNAL ID
TABLE 4-20

Digital Format	ID
H	High-True Logic Level
L	Low-True Logic Level
L1/L2	Two signals with same mnuemonic but with logic levels L1 and L2.
L1→L2	Signal asserts action on transition from L1 to L2.
L1↔L2	Pulse train between logic levels L1 and L2. (May be symmetrical or with no predefined periodicity.)
F1:F2	Sequence from logic function F1 to logic function F2 that is indicated by a ":". (Complex functions may be enclosed in "< >".)
XOR	Exclusive "or"
OR	Inclusive "or"

DIGITAL FORMAT ID
TABLE 4-21